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THESIS:

AN EXPERIMENTAL INVESTIGATION AND DESIGN OF A DIGITAL TELEMETRY ACOUSTIC RECEIVING ARRAY

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AN EXPERIMENTAL INVESTIGATION AND DESIGN OF A DIGITAL TELEMETRY ACOUSTIC RECEIVING ARRAY

BY

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THESIS

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DEDICATION

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ABSTRACT

AN EXPERIMENTAL INVESTIGATION AND DESIGN OF A DIGITAL TELEMETRY ACOUSTIC RECEIVING ARRAY

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Acoustic Receiving Line Arrays are critical tools for measuring the acoustic properties of any oceanographic region. Vertical, horizontal, and combinations of the two array configurations allow us to measure acoustic propagation, bottom characteristics through inversion, and ambient noise. These properties are vitally important for effective implementation of any passive or active detection system in both shallow and deep water environments. Measurement systems must be designed with flexibility since the exact array design that yields the best signal processing results is not known prior to a survey. Flexibility, in this case, refers to large numbers of hydrophones, higher sample rates for greater bandwidth, and longer recording time to facilitate experimentation at each survey site. Repeated deployment and recovery of such a system demands a battery powered autonomous design that can be deployed and recovered from available research vessels at

sea. Conventional deep ocean analog array cable designs, while power efficient, become physically challenging in size and weight when the sensor count exceeds 100 and array lengths remain in the 100s of meters. The purpose of this thesis is to detail the design, development, and testing of a pressure tolerant full ocean depth rated prototype acoustic line array with digital telemetry of all hydrophone data from the sensors to the recording system. The design is to support up to 300 hydrophones each with a maximum sample rate of 4 kHz and a per sensor power requirement of ¾ of a watt. Lower sensor counts will allow higher sample rates to be used based on available telemetry bandwidth. A single element of a line array was built and tested at the University of Texas at Austin Applied Research Laboratories and it was used to demonstrate real-time telemetry and recording of acoustic hydrophone data.

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CHAPTER 1 INTRODUCTION

1.1 BACKGROUND

"Acoustics, particularly underwater acoustics, is not a very precise science [1]." Indeed the ocean is an unfavorable environment due to its constantly changing state, extreme depths and pressures, and corrosive nature. Yet there are still many scientific, commercial, and military sensing applications that necessitate the engineering and development of acoustic measurement devices capable of operating in these conditions with reasonable accuracy. The primary push for development of underwater electro-acoustic transducers came from Navy sonar system applications during World War I. The emphasis placed on such research at the time led to great advancements in transducer design and calibration with contributions from then Bell Telephone Laboratories, Columbia University Division of War Research, Harvard Underwater Sound Laboratory, University of California, Massachusetts Institute of Technology, and other Navy Research Laboratories. Post war funding drops resulted in the withdrawal of many institutions from underwater transducer research and the Navy was given responsibility for overseeing the university-managed laboratories. The University of Texas at Austin has operated a University Affiliated Research Center or UARC since it was originally created as Defense Research Laboratory in 1954. Now called Applied Research Laboratories (ARLUT), the laboratory continues its long history of contributing to the development and testing of advanced underwater passive and active measurement systems.

Hydrophone line arrays have long been used as a means of improving receive capability over a single hydrophone with regard to achievable gain and directivity. Signal processing techniques, such as beamforming, use contributions from each

individual hydrophone in order to emphasize received signals from a particular look direction. Proper phase manipulation in the time domain, or more often the frequency domain, can result in receiver gain in a particular look direction while providing some rejection of un-wanted noise in other directions. While there are many advanced topics on beamforming beyond the scope of this thesis, line arrays are a useful tool for sensing in both deep and shallow water environments. They can be used to evaluate the acoustic propagation characteristics of a particular area and then used operationally to take advantage.

ARLUT has developed a number of acoustic measurement systems for shallow and full ocean depth applications. Both horizontal, vertical, and combination arrays have been constructed and successfully deployed. Historically these arrays are analog in design with individual twisted pair wires for each hydrophone. An analog approach is power efficient, low cost, easy to manufacture, and provides redundancy. While the analog design has been successful, the need for larger element counts in the array designs is driving a push for digital telemetry arrays that multiplex hydrophones over fewer conductors. An analog design becomes impractical beyond 100 or so hydrophones for arrays that are hundreds of meters in length. The physical size of the cable is the limiting factor. Multiplexed designs have been used previously in Navy sonobuoy applications as well as towed arrays. Most cases in which digital arrays were used involve very small lightweight drifting buoys, towed arrays with virtually unlimited power, or fixed installations again with few power limitations and relaxed deployment requirements. Field deployable survey arrays designed to be recoverable and flexible in their design must be rugged enough to survive and be re-deployed, cost effective enough to be feasible, and low power enough to allow for week long or longer data collections. The

development of a telemetry architecture that conforms to this goal is important in realizing a transition away from the analog designs.

1.2 Research Objective

The primary focus of this thesis is to investigate current industry digital telemetry hardware, identify a cost effective technology solution using off the shelf components, and design and develop a prototype digital telemetry array (DTA). While digital data is common today and availability of transmission media is widespread, there are design factors particular to array construction that make many options impractical. Splicing requirements and complexity, power consumption, transmission distance, processing overhead, and cost are all determining factors. Fiber optic cable is difficult to splice when compared with copper wire, has certain bend radius limitations and fragility, and its multi-kilometer long distance signaling capability may not be necessary. A solution is desired that accommodates cost effective fabrication techniques that involve splicing acoustic hydrophone elements into a submersible cable at multiple locations. Physical size should be kept to a minimum to accommodate future packaging and deployment needs. Ultimately, a pressure tolerant electronics design is important in eliminating the need for a pressure vessel at each acoustic node location. Element counts up to 300, array lengths up to 400 meters without a repeater, and per element power consumption of ¾ of a watt or less are required. The telemetry design must accommodate 16 bit resolution sampling with an acoustic bandwidth of 4 kHz.

1.3 Outline of Thesis

Chapter 2 presents the design concepts and theories relevant to the development of a digital telemetry full ocean depth pressure tolerant acoustic line array. An emphasis is placed on hydrophone selection and amplifier design for achieving a desired system

self noise and receive sensitivity targeted for deep ocean environments. Analog to digital converters, a local DSP for programmability, power distribution, timing schemes, and finally, digital telemetry schemes and hardware interfaces are discussed.

Development of a single acoustic element prototype is covered in chapter 3. Hardware design begins with the use of manufacturer development kits to evaluate telemetry transceiver and DSP interfacing and performance. The selection of each hardware component and the corresponding design is discussed through fabrication of an initial and final custom prototype acoustic element. Assembly of a data recorder, array interface module, array cable, and element encapsulation potting mold are also described.

Chapter 4 examines the experimental testing, and corresponding results, performed throughout the prototype development. The selected hydrophone element and chosen printed circuit board (PCB) form-factor are evaluated via measurements with an acoustic model prototype. Amplifier, A/D, DSP, and telemetry performance are all evaluated. Pressure tolerance testing is performed on individual electrical components as well as the entire potted prototype element. Pressure effects on the impedance of coaxial cable at depth are investigated and measured. Finally, an acoustic data collect is performed to evaluate the completed element's receive sensitivity and frequency response.

A summary of the results is presented in Chapter 5.

CHAPTER 2 HARDWARE DESIGN

Oceanographic hardware design requires the use of multiple disciplines in order to address the challenges of extreme hydrostatic pressures, corrosion, motion induced fatigue, temperature variations, and an overall unforgiving environment. This section provides a general discussion of important design considerations, theories, equations, and driving factors that determine how best to select the appropriate technologies and identify a suitable design for each hardware category associated with a deep ocean acoustic array.

2.1 HYDROPHONE DESIGN

Hydrophones represent a subset of transducers designed specifically to operate underwater for acoustic sensing applications. While the range of transducer types employed in the construction of hydrophones does vary, piezoelectric ceramic based transducers are certainly predominant in receivers and are quite common in transmitters and actuators as well. Piezoelectric ceramic materials are economical to manufacture, can be formed into custom shapes, have good stability over time, and its electromechanical properties can be designed accurately using theoretical models. A complete discussion of piezoelectric transducer design is beyond the scope of this thesis. Full ocean depth rated transducers must operate in ambient pressures exceeding 68.9 MPa. Deep water environments often impose additional requirements for higher sensitivity and low self noise due to the inherent volumetric spreading loss and low ambient noise as compared to a littoral zone.

2.1.1 Hydrophone Form Factor

Air backed cylindrical and spherical piezoelectric transducers are the most commonly used for hydrophone applications. They can be manufactured in a variety of

sizes and electrode configurations and are widely available commercially. The air backed cylinder requires end caps to be applied in order to maintain the air backing when used under hydrostatic pressure. Both types require encapsulation for waterproofing. The air backing allows the ceramic material to flex and retain its sensitivity even under extreme pressures. Hydrophones are typically designed for operation below their resonance, yielding a flat omnidirectional response over a wide frequency range. Ultimately, the size of the transducer will depend on the desired frequency of operation, sensitivity, and form factor of the desired receiver.

2.1.2 Hydrophone Free Field Voltage Sensitivity

A few conditions should be imposed in order for the following discussion to be simplified and narrowed to address this specific application. In general, piezoelectric transducers are used as pressure sensing hydrophones, meaning that they convert free field pressure amplitude into an output voltage proportional to its sensitivity. Directional effects as well as frequency dependence can often be neglected when operating well below resonance and for large wavelengths relative to the physical dimensions of the transducer. In this regime, the plane wave pressure amplitude is uniform across all transducer surfaces. The hydrophone free field voltage sensitivity is then defined as the ratio of open circuit voltage output to free field pressure amplitude input and is expressed in units of dB re 1V/µPa. Although it is not often explicitly written in underwater acoustics, these are measured rms quantities. The true sensitivity of the transducer is based upon its piezoelectric constants and coupling coefficients that pertain to the direction of applied acoustic pressure relative to the polling axis of the ceramic. Material selection for desired coupling coefficients, which relate applied stress to electric field generation, and proper polling to leverage a particular flexural mode are two fundamental

factors driving transducer design. Given the commercial availability of high quality transducers, an array designer can purchase a hydrophone with specified sensitivity and operating depth ratings beyond 6000 meters. All piezoelectric transducers produce thermally generated output voltage noise due to their equivalent series impedance in addition to the signal of interest. The self noise of any array element needs to be less than the ambient noise for the intended environment and includes contributions from the hydrophone, the preamplifier, and the analog to digital converter. Given the availability of very low noise amplifiers today, the hydrophone self noise is often dominant and must be considered during selection. Section 2.1.4 addresses calculation of piezoelectric hydrophone self noise. Next we will discuss a basic equivalent circuit for piezoelectric transducers used to model its electromechanical response and noise characteristics.

2.1.3 Hydrophone Equivalent Circuit

It is customary in pressure sensitive hydrophone design to use the impedance analog to develop an equivalent circuit. Figure 2.1 accounts for the acoustic and mechanical elements coupled to the electrical elements via an ideal transformer whose turns ratio, N, is proportional to the transduction coefficient. Electrical voltage is analogous to mechanical force and electric current is analogous to mechanical velocity. R_r and M_r represent the acoustic radiation impedance; F_b is the force acting on the hydrophone surface of area A due to the uniform incident acoustic pressure; M and R represent the mechanical mass and resistance of the piezoelectric ceramic itself; C^E represents the mechanical compliance; and G_o and C_o are the electrical shunt conductance and capacitance of the transducer, where G_o is defined by,

$$G_o = \omega C_f \tan\delta \tag{2-1}$$

where $\tan\delta$ is often referred to as the dissipation factor or loss tangent.

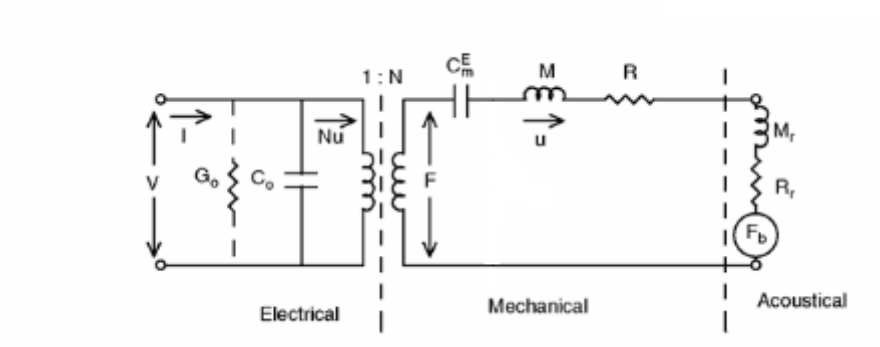

Figure 2.1: Lumped Equivalent Circuit ([2], Figure 2.11 with tail mass removed)

For frequencies well below resonance, often referred to as the stiffness region, the mechanical compliance dominates the impedance $1/j\omega C^E$ and the equivalent circuit can be replaced with that of Figure 2.2. A typical air backed cylindrical transducer used to measure frequencies below 4 kHz and whose physical dimensions are on the order 1" diameter by 2" in length certainly falls within this category. The transformer can be removed and the compliance C^E and acoustic force F_b become N^2C^E and F_b/N respectively.

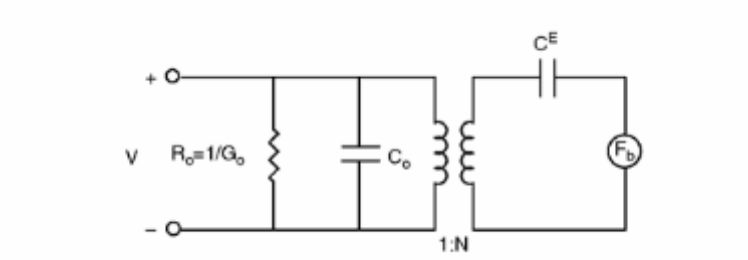

Figure 2.2: Low frequency hydrophone equivalent circuit ([2], Figure 4.3)

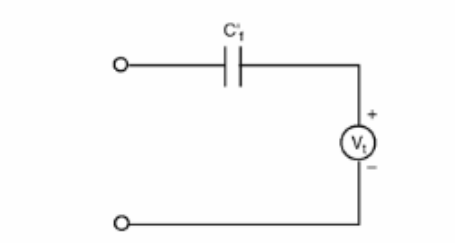

Figure 2.3: Thevenin equivalent circuit representation ([2], Figure 4.4)

In Figure 2.3, from [2]

$$V_t = k^2 F_b / [N(1 - j\tan\delta)] \tag{2-2}$$

where

$$k^2 = N^2 C^E / C_f \tag{2-3}$$

and

$$C_f^{'} = C_f(1 - j\tan\delta) \tag{2-4}$$

2.1.4 Hydrophone Self Noise

In this stiffness region of operation well below resonance and anti-resonance, the internal thermal Johnson noise is dominated by the equivalent dissipative resistive part of the electrical impedance $1/j\omega C_f$, which is from [2],

$$R_h = \text{Real}\{1/j\omega C_f(1 - j\tan\delta)\} = (\tan\delta/\omega C_f)/(1 + \tan^2\delta) \approx \tan\delta/\omega C_f, \tan\delta << 1 \tag{2-5}$$

This real resistance determines the mean squared noise voltage by,

$$\langle V_n^2 \rangle = 4kTR_h\Delta f \tag{2-6}$$

where k = Boltzmann's constant ($1.381\text{x}10^{-23}$ Joule/Kelvin), T is the absolute temperature, and Δf is the bandwidth. At 20˚C,

$$10\log_{10}\langle V_n^2 \rangle = -198\text{dB} + 10\log_{10} R_h + 10\log_{10}\Delta f \tag{2-7}$$

We need to convert the noise voltage to an equivalent mean-squared noise pressure using the hydrophone's sensitivity M(V/μPa).

$$10\log_{10}\left\langle p_n^2 \right\rangle = -198\text{dB} + 10\log_{10} R_h - 20\log_{10} M + 10\log_{10} \Delta f \tag{2-8}$$

At higher frequencies, the mechanical resistance and radiation resistance must be included in the calculation of thermal Johnson noise. For the purposes of this array design, those effects are negligible. Given a hydrophone's specified sensitivity, free capacitance, and dissipation factor, the expected self noise due to Johnson thermal noise can now be estimated. If the equivalent series resistance is too great or the bandwidth large enough, the self noise may limit the overall noise floor of the system. These effects are most pronounced at low frequencies, for hydrophones with low capacitance (potentially small in size), and for piezoelectric types that have a high dissipation factor which normally ranges from 0.004 to 0.02. Section 3.1.1 illustrates the application of these formulas to an HTI-94-SSQ model hydrophone for the prototype array development covered by this thesis. Commercially available admittance, low frequency capacitance, and dissipation factor meters allow for direct measurement of the necessary parameters to populate the equivalent circuits shown here. The capacitance and dissipation factor measurements are usually performed at 1 kHz in air. The determination of the necessary lumped element parameters from these measurements is beyond the scope of this thesis, but it is important to note that they are readily attainable with the proper equipment.

2.2 Amplifier Selection & Design

For low noise deep ocean applications, signals of interest are often low amplitude due to spreading loss and attenuation over long range propagation paths. In an effort to keep the receiving hydrophone's physical size down, we have to settle for limited sensitivity. Air backed PZT cylindrical hydrophones of the dimensions discussed earlier often vary around -195 dB re 1 µPa sensitivity. Some manufacturers offer hydrophones with built in pre-amplifiers for higher sensitivities. In order to increase the hydrophone output to a level large enough to fit within the smallest quantization bin of an A/D converter, a large amount of gain is often required between the transducer and the converter. The requirements for the system noise floor may be determined based on the desired operating environment. From Figure 2.4, the ambient noise in deep water for sea state zero (SS0) is around 45 dB re 1µPa. Measurement of signals just above the ambient noise level is usually the design objective for each individual hydrophone in passive applications. The required dynamic range is based upon the difference between the smallest signal of interest and the largest. A 16 bit A/D converter provides 90 dB of dynamic range and is usually adequate for most underwater acoustics receivers. The 16 bit A/D provides only 90 dB of dynamic range because the acoustic signals are bipolar and must swing positive/negative, which halves the range of the converter. Assuming the designer has selected a hydrophone with self noise levels below SS0, and wishes to measure signals as small as 45 dB re 1µPa, the amplifier gain selected must map the hydrophone output into the A/D voltage range. Too much gain will waste lower order quantization levels filling them with noise, while too little gain will fail to map the small signal response into the lowest order bins at all. These parameters drive the amount of gain required and must be considered together.

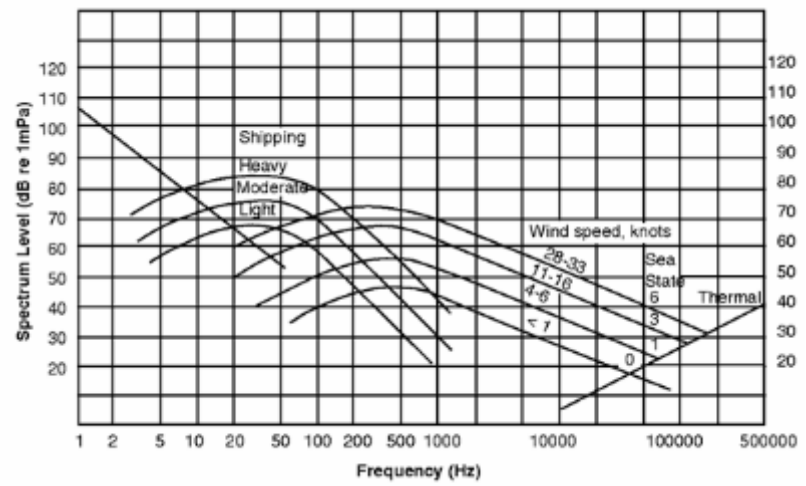

Figure 2.4: Average deep water ambient-noise spectra, where mPa refers to µPa ([3] Fig 7.5)

2.2.1 Amplifier Configuration

Piezoelectric transducers are charge coupled devices and require high input impedance amplifiers in order to avoid loading down their response. Instrumentation amplifiers offer very high impedance differential inputs with excellent common mode rejection well suited for PZT transducers. These amplifiers come in pre-packaged ICs or can be customized using individual operational amplifiers.

2.2.2 Single Voltage vs. Dual Rail Supply

The use of single supply voltages in amplifier designs has become more common with the popularity of low power battery operated devices. Lower voltages decrease power consumption in mobile processors and eliminate the need for a negative supply rail simplifying the overall system design and improving efficiency. Single positive supply instrumentation amplifiers are available. Given their differential inputs, this does not impose any new requirements on the transducer connection. The amplifier output, however, does need to remain differential or be biased in between the positive rail and common. Dual rail supply instrumentation amplifiers have been used extensively for

decades and are quite common. The disadvantage is obviously the need for a negative power supply rail.

2.2.3 Single Ended vs. Differential

Utilizing differential signals throughout the amplifier design should be a goal whenever possible. For transducer amplifiers with large amounts of gain, vulnerability to electronic noise in the lab is a real problem for single ended designs, especially 60 Hz EMI. These noisy interference signals are not usually a problem when the hydrophones are deployed underwater away from noise sources, but pose a major headache during laboratory test and measurement. The transducer outputs can be treated as differential signals fed directly to the inputs of an instrumentation amplifier. The common mode rejection will strongly reduce any EMI that would otherwise be picked up and amplified. The amplifier output can be maintained as a differential signal driven directly into differential inputs at the A/D converter.

2.2.4 Input Self Noise

All operational amplifiers generate unwanted output signals in the form of noise that can come from the amplifier itself, components in the feedback loop, the power supply, or be induced in the input, output, ground, or measurement circuit from outside sources [4]. For interference sources, the primary course of action is to apply filtering, decoupling, or shielding to minimize or eliminate the noise. Electronic interference is less likely in most underwater acoustic receivers located far from any other electrical devices; however, mechanical noise from cable strum and wave action as well as flow noise are noise sources that must be considered. For random uncorrelated noise associated with silicon devices, such as Johnson thermal noise, Schottky noise, Flicker noise (1/f), and Popcorn noise, it is appropriate to characterize the noise with an rms

value. This provides a simple single value representation of the noise including contributions from the entire frequency band.

$$E_{rms} = \sqrt{\frac{1}{T}\int_0^T e^2\,dt} \tag{2-9}$$

where

E_{rms} = RMS voltage value

T = Measurement interval

e^2 = Instantaneous noise votlage

Given that the amplifier noise may vary as a function of frequency and we may be interested in operation of a subset of the frequency band, it is often more useful to express the noise as a spectral noise density, e_n, as defined in [4]. We can now express the rms noise value, E_n, for a given frequency band as the square root of the definite integral of the square of spectral noise density.

$$e_n^2 \equiv \frac{d}{df}\left(E_n\right)^2 \qquad (2\text{-}10) \qquad\qquad E_n = \sqrt{\int_{f_1}^{f_2} e_n^2\,df} \tag{2-11}$$

The Johnson noise voltage within a bandwidth Δf as seen earlier is given by,

$$E_{rms} = \sqrt{4kTR\Delta f} \tag{2-12}$$

By inspection of equation 2-11, we can see that e_n, for Johnson noise, is $\sqrt{4kTR} = 0.13\sqrt{R}$ (μV/$\sqrt{\text{Hz}}$) at room temperatures and is a constant. To calculate the rms Johnson noise voltage over a given frequency band, we need only multiply by the bandwidth of interest.

The total RMS noise due to uncorrelated noise in different portions of the frequency spectrum is calculated by adding the square root of the sum of the squares of each individual contribution. Op amps now have input referred spectral noise density levels in the 5 to 1 nV/√Hz range from 10Hz to 1 kHz respectively. It is often the thermal noise generated by the source resistance and feedback resistors that contribute the majority of the noise. By summing the input referred amplifier self noise with the transducer self noise and applying the appropriate amplifier noise gain we can calculate the total self noise at the A/D converter.

2.3 Analog to Digital Converter

Traditional sampling A/D converters, like successive approximation, sample and hold, etc. have been replaced in many applications recently by delta-sigma converters. The basic functionality of this type of converter consists of two primary components: a modulator and a digital filter. The modulator samples the input signal together with a reference voltage to produce a 1's density output stream. The output stream density is proportional to the analog input level relative to the reference voltage. The pulse stream leaves the modulator and is then processed by a multi-stage FIR digital filter where the output sample conversion is produced [5]. The analog input signal and reference voltage are sampled at a high rate, typically 64 times the final conversion rate, which causes the quantization noise to be shifted into higher frequencies. This noise shaping allows the following digital filter to remove a large portion of the quantization noise resulting in low noise passband output. The oversampling within the modulator also has the added benefit of relaxing the requirements on the anti-aliasing filter since aliasing will not occur until the input signal frequency approaches the modulator sampling frequency. This allows for the use of a simple single pole anti-alias filter. Delta-Sigma converters are

available with multiple simultaneously sampled channels per IC, linear phase response, differential inputs, and single supply rail operation requiring as little as 7mW per channel for low sample rate applications below 10 kHz. Data may be read from the converter over a serial interface, such as a SPI port, allowing for easy integration with a local processor. The advantages over traditional A/D converters make delta-sigma converters a good choice for low power transducer designs.

2.4 TIMING SCHEMES

There a few different clocks required to satisfy the acoustic sample timing, telemetry timing, and individual node local processor core functions. A master acoustic sample clock can be driven down the array to each element allowing for synchronized sampling. Propagation delay down the cable represents the only inter-element sample delay and is often negligible. This can be accomplished using a differential serial line driver IC, such as an RS-422/485 driver, originating the in the primary recording/control system. This requires a dedicated twisted pair and can support clock rates in the 5-10MHz range over cable lengths up to 100 meters. Clearly lower clock rates will support longer cable lengths due to decreased high frequency rounding and attenuation of the clock pulses. High impedance serial receiver ICs allow for up to 300 receivers to tap onto the same clock line without excessive loading, making it possible to share a single clock wire pair.

For a multiplexed digital telemetry bus to support hundreds of acoustic elements sampled at 4 kHz with 16 bit resolution, the transceivers must operate in the 10s of MHz in order to provide adequate bandwidth. Most commercial line driver transceivers will accept a master clock in addition to transmit and receive clocks which drive a serial data interface. The master clock may be generated using a local oscillator, however, the

transmit clock is generated by the local processer's serial port acting in the master mode while the receive clock is typically generated by the transceiver itself and is often the product of a clock recovery circuit that phase aligns with the incoming data.

The local processor requires a core clock to function. This clock needs to be sourced with a local oscillator and does not necessarily need to be at the core operating frequency due to clock multipliers within the processor. For a pressure tolerant design, standard crystal oscillators are not acceptable since they contain air pockets within the case and will crush under pressure. The availability of three terminal silicon oscillators that need only power and common to provide a square wave clock offers a pressure tolerant solution and make excellent core clocks.

2.5 EMBEDDED PROCESSOR

A number of trade-offs must be weighed in the selection process. Core speed, power consumption, peripherals, memory, and programming tools are the primary factors worth consideration. There are very powerful communications processors designed to interface with line driver transceivers built with functionality to support standardized protocols. While these processors, such as the Motorola PowerQUICC series, would seem like a perfect fit, they are often designed to act as point to point processors within network hubs. The same can be said for many of the physical layer devices, like framers, that may be placed in between a processor and a transceiver. They are multi-featured but require large amounts of power, which would normally not be an issue for a network hub on AC power handling a point to point link. In a battery powered autonomous array where each element must interface with a telemetry link, requiring a processor and transceiver at each node, power must always be minimized. This constraint motivates the desire to find a general purpose low power processor that can be interfaced with a low

power physical layer transceiver. For arrays with close element spacing, 1 to 1.5 meters, multiple hydrophone elements could be run to a multiplexer node where digitizing occurs along with the telemetry interface. This would allow for a reduction in the total number of processors and transceivers in the array. For a design that is not constrained by inter-element spacing, fully functional independent element nodes with long range high speed transceivers offer the most flexibility at the cost of power consumption. The later is the approach taken in this thesis given the intent of designing a general purpose research tool suitable for any as yet undetermined array dimensional requirements and complete element interchangeability.

Analog Devices, Texas Instruments, Altera, Xilinx, and many other manufacturers offer a range of processing solutions ranging from basic general purpose processors and microcontrollers to low power FPGAs. As mentioned earlier, in order to interface with transceivers and A/D converters, at least two SPI ports and two SPORTs are desirable and are readily available on standard products from the manufacturers referenced above. FPGAs are attractive for their low power operation, flexibility in generating serial interfaces to support peripherals, and availability of IP cores to support telemetry protocols like Ethernet. The additional complexity of programming FPGAs must be considered but is becoming less demanding with the improvement of Integrated Development Environments with higher level graphic utilities. For ease of programming and flexibility, a general purpose Digital Signal Processor (DSP) was selected for this thesis project from Analog Devices Blackfin line of processors. On board Flash memory allows for program storage without the need for external Flash or SRAM IC integration simplifying the PCB design and programming requirements. While power consumption may not be the lowest available for the given functionality requirements, the capabilities

compliment a general purpose re-programmable design. For more permanent designs, an FPGA would likely be ideal.

2.6 Power Distribution

For lengthy array cables, the resistive losses can become considerable as the current draw increases and are referred to as I^2R losses. In order to minimize those losses it is necessary to drive higher voltage down the array and then step it down to the required 5V, 3.3V, and lower voltages required by the hydrophone element analog front end, A/D converter, processor, and transceiver. Reasonably high power conversion efficiencies in the 85-90% range can be achieved with DC-DC switched mode power supplies that can accept wide input voltage ranges from 18-72 volts. The conversion is typically less efficient as the difference between the input voltage and the output voltage increases. Also, switched mode supplies are often more efficient when operated at the high end of its rated output power and less efficient when run at low power. Manufacturers such as Calex, Gaia, Linear Technologies, and many others offer full ranges of switched mode power supplies for various power requirements and in various package types. Increasing the gauge of the power wires, as well as doubling up on the number of pairs carrying power, will help reduce losses in the array cable. For short duration array deployments, individual battery powered hydrophone nodes could be employed. For multi-week deployments, and certainly for a general purpose design aimed at flexible operating times, a DC-DC converter approach leveraging centralized power sourced from the main electronic recording system's battery's and sent down the array is the desired approach.

2.7 DIGITAL TELEMETRY

The objective is to develop a telemetry system based on long distance, baseband, relatively high bandwidth, and twisted pair copper or coaxial wire telecommunication industry technology. The telecommunications industry has adopted a standard hierarchy for combining different sources into a high-speed digital TDM signal for transmission over various networks. This standard hierarchy is shown in below.

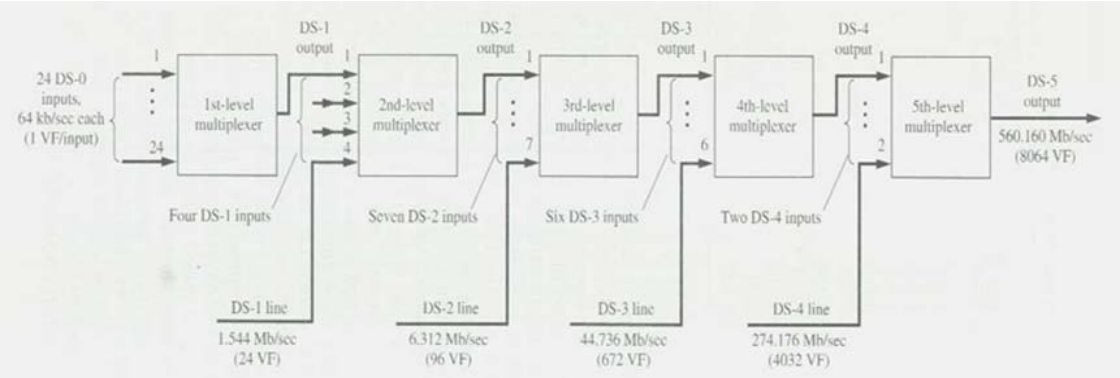

Figure 2.5: North American Digital TDM Hierarchy [6]

The standardized time division multiplexed hierarchy needs to be adapted to a multi-drop long distance shared bus topology. Fiber Optic based physical layer designs require too much power, introduce far too much complexity due to the need for re-termination of the fiber at every single node, and are somewhat fragile physically imposing bend radius limitations. The use of copper based transmission media simplifies the array construction, reduces cost, and allows the use of lower power hardware. Given the long standing history with copper cabling in the telecommunications industry, the achievable data rates for various wire types are well known as shown in Table 2-1.

Digital Signal Number	Bit Rate, R (Mbits/sec)	No. of 64 kbits/sec PCM VF Channels	Transmission Media Used
DS-0	0.064	1	Wire pairs
DS-1	1.544	24	Wire pairs
DS-1C	3.152	48	Wire pairs
DS-2	6.312	96	Wire pairs, fiber
DS-3	44.736	672	Coax., radio, fiber
DS-3C	90.254	1344	Radio, fiber
DS-4E	139.264	2016	Radio, fiber, coax.
DS-4	274.176	4032	Coax., fiber
DS-432	432.00	6048	Fiber
DS-5	560.160	8064	Coax., fiber

Table 2-1: TDM Standards for North America [6]

Each type of digital transmission is next referred to as a specific T-Carrier system based on the transmission medium and line code used in the actual implementation. Table 2-2 shows the T-Carrier specifications for baseband digital transmission systems. The T3 transmission system possesses adequate bandwidth to support at least 300 nodes using the DS3 44.736 MHz signaling. Transmission over 385 meters is possible over coax, and individual line interface units (LIUs) are available from multiple vendors. The next step is to define a network protocol to run over a DS3 data link.

System	Rate (Mbits/s)	System Capacity: Digital Signal No.	System Capacity: Voice Channels	Medium	Line Code	Repeater Spacing (miles)	Maximum System Length (miles)	System Error Rate
T1	1.544	DS-1	24	Wire pair	Bipolar RZ	1	50	10^{-6}
T1C	3.152	DS-1C	48	Wire pair	Bipolar RZ	1	—	10^{-6}
T1D	3.152	DS-1C	48	Wire pair	Duobinary NRZ	1	—	10^{-6}
T1G	6.443	DS-2	96	Wire pair	4-level NRZ	1	200	10^{-6}
T2	6.312	DS-2	96	Wire pair[a]	B6ZS[b] RZ	2.3	500	10^{-7}
T3	44.736	DS-3	672	Coax.	B3ZS[b] RZ	[c]	[c]	[c]
T4	274.176	DS-4	4032	Coax.	Polar NRZ	1	500	10^{-6}
T5	560.160	DS-5	8064	Coax.	Polar NRZ	1	500	4×10^{-7}

[a] Special two-wire cable is required for 12,000-ft repeater spacing. Because T2 cannot use standard exchange cables, it is not as popular as T1.

[b] BnZS denotes *binary n-zero substitution*, where a string of n zeros in the bipolar line code is replaced with a special three-level code word so that synchronization can be maintained [Fike and Friend, 1984; Bic, Duponteil, and Imbeaux, 1991].

[c] Used in central telephone office for building multiplex levels; not used for transmission from office to office.

Table 2-2: Specifications for T-Carrier Baseband Digital Transmission Systems [6]

Network protocols introduce additional overhead into the telemetry link, but their advantages include error tracking, addressability of connected nodes, and standardized packetizing of the data. Packet switched network protocol such as Asynchronous Transfer Mode (ATM) are connection oriented, utilize virtual circuits, fixed byte packet cells, and can be run over a DS3 link. Ethernet is a widely used carrier sense multiple access shared link network topology. 10BASET and 100BASET Ethernet can be run over relatively long runs of category V twisted pair communication cable. According to [6], Ethernet taps must be a minimum of 2.5 meters apart, which would limit the hydrophone element spacing if they were to be truly tapped into the transmission line. Each node would need an Ethernet transceiver and would be assigned an IP address and Ethernet media access controller (MAC) address. As long as the bandwidth is adequate and the inter-element spacing is not an issue, nodes would be queried in turn for data requiring a request/response transaction for each node. Again, if the additional overhead does not pose a problem, this approach would be acceptable. For array configurations in which multiple hydrophones are digitized at a multiplexer node, it is more efficient to use Ethernet to transmit the multiplexed data than in an individual case. Ethernet protocols are now easily implemented in processors and FPGAs. For the purposes of this thesis, the array hydrophone nodes are designed for daisy chain connections. Each element communicates its data to the next element, which then adds its data and re-transmits the data to its neighbor, reconditioning the signal in the process. Design steps are employed and discussed to address vulnerabilities with this approach in Chapter 3. In this scheme, simple data transmission from one point to the next does not necessarily require a complex protocol. It is simple enough to implement a basic packet with a header, data payload, and tail for accommodating commands and array data. For that reason, simple DS3 transceivers in conjunction with the BlackFin DSP using a basic packet type were

selected for this thesis. A standard protocol could replace the custom packet as well as an Ethernet transceiver for future designs.

2.8 Data Recorder

The data recorder will be contained in an instrumentation pressure vessel (IPV) that protects it for deep ocean deployments. The hydrophone array connects to the recorder inside the IPV through a special sealed bulkhead connector. Previous Applied Research Laboratories Environmental Sciences data recording systems were based on National Instruments PXI form factor embedded CPUs, data acquisition, and data storage cards. The objective of this thesis is to leverage the same recorder design and hardware whenever possible to maintain compatibility. Alternative designs could incorporate PC-104 form factor CPUs and DAQs for example. The ability to program the recorder using LabVIEW is an advantage when working with limited time or funds allowing for rapid software development and testing. The data recorder will interface with the array via a parallel I/O connection. This will allow for 16 bit data sample transfers at high speed. USB or Ethernet could be used; however, the parallel connection can use existing LabVIEW drivers and BlackFin DSP API functions without additional driver development. Data will be stored on 2.5” laptop hard drives contained in IDE to USB drive carriers and will connect to the PXI CPU via USB connection.

2.9 Array Interface Module

In order to send/receive commands and receive data from the array, a suitable interface must be designed. This hardware must include a mating transceiver and processor for converting commands and data to/from array telemetry signaling. The AIM must also incorporate an interface for data transfer to the recorder. As mentioned in section 2.8, there are a number of interfaces that may be used. A parallel I/O port is used

rather than Ethernet in this thesis for simplification of the interface programming. The array sample clock signal source can be incorporated into the interface module electronics box. For redundant designs with multiple sets of array telemetry buses, there would naturally need to be multiple sets of transceivers, however a shared processor for data de-multiplexing and array command/control could likely be used.

2.10 Pressure Tolerant Design

The specified requirement for full ocean depth operation imposes an additional design complication for the electronics as well as the hydrophone, physical array cable, recording system, and batteries. In many cases, the signal conditioning and digitizing electronics are located inside specially designed pressure vessels that protect the electronics from contact with seawater and pressures in excess of 55.1 MPa. For many analog array designs, most if not all of the electronics can be located inside the primary recording system pressure vessel, with perhaps the exception of a hydrophone preamp that can often be built inside the air backed hydrophone itself. Digital array designs may employ a number of pressure vessels distributed throughout the array where multiple analog acoustic channels are multiplexed. One of the primary objectives of this thesis was to generate a design in which all of the array components, including signal conditioning, digitizing, and digital telemetry, are pressure tolerant. This eliminates the need for pressure vessels reducing cost, size, and weight, simplifying construction, and minimizing the number of leak paths associated with o-ring interfaces. Section 2.10 covers various electronic and mechanical component types, hardware preparation and encapsulation techniques, and pressure testing methods/requirements that have proven to be effective for deep ocean pressure tolerant designs.

2.10.1 Component Selection

Critical to the success of a pressure tolerant circuit is the selection of the right types of electrical components. Oil filled housings are commonly used to protect electronics in marine applications. The oil also serves to penetrate underneath electronic components and to fill air gaps as the pressure increases. Air pockets are the root cause of most electronic failures at pressure. Air pockets exist beneath socket and surface mount components, inside electrolytic capacitors, and within ceramic ICs. Inductors with very sensitive construction may be affected by removal of the air core, changing the magnetic permeability and detuning critical circuits. These issues are further complicated when using a urethane to encapsulate the hardware instead of oil. Urethanes typically posses a much higher viscosity during the molding process and likely will not fill all air gaps. Array cables can be designed using many different materials and architectures. There are sealed designs, flooded designs, and designs with widely varying requirements for conductor types and numbers.

2.10.1.1 Hydrophones

Given the wide range of transducer shapes used to design hydrophones, it is meaningful to point out those families that are well suited and those that are sure to fail at depth. In many low power small physical size hydrophone applications, an air backed approach is used to increase the transducers sensitivity. The nature of the air chamber and the transducer design must be analyzed in order to determine the pressure rating and the effect of pressure on the hydrophone's sensitivity within its operational depth range. Shallow water omnidirectional hydrophones used in Navy sonobuoys use an air backed circular bender element. The piezoelectric element is mounted on top of a dished metal backing plate, creating an air pocket. These hydrophones have good sensitivity when used above 300 or 400 meters. Beyond that depth, the pressure on the ceramic element's

face will eventually cause it to crack and fail. Spherical and cylindrical piezoelectric hydrophones can be manufactured with adequate wall stiffness to not only survive full ocean depth pressures, but to retain their sensitivity with good precision throughout the water column. These hydrophones can be built with preamplifiers installed inside the element prior to installation of the end caps or mating of the hemispheres and are excellent choices for omnidirectional applications.

2.10.1.2 Electronic Components

As mentioned preciously, there are a number of basic circuit component types that are not suitable for pressure tolerant designs due to the presence of internal air pockets. Ceramic ICs have been found to fail pressure tests when immersed in castor oil due to this vulnerability. Electrolytic capacitors are manufactured in such a way that micro voids throughout the rolled anode-cathode electrolyte construction allow compression and internal shorting to occur. Tantalum, ceramic, and plastic capacitors, in general, have performed well in pressure tests up to 68.9 MPa. Plastic ICs, surface mount or socket, to include basic op-amp, CMOS logic, A/D converters, DSPs, FPGAs, transistors, voltage references, etc. have also successfully passed pressure testing. This is not to say that all such components will pass, but rather that each selection must be tested in order to verify suitability, but that those families of components are highly likely to be pressure tolerant. Transformers, DC-DC switching supplies, and other specialty components must each be vetted independent of this discussion.

2.10.1.3 Array Cables

The physical array design lies at the heart of both vertical and horizontal array designs. Clearly, power, data, and clock signals must be incorporated and the designer must select the appropriate number of conductors, wire gauge, wire type (twisted pair,

coax, shielded or unshielded), and wire insulation type. Depending on the array design, the cable may be required to undergo considerable mechanical load and tension, perhaps to support floatation. This may require the incorporation of a strength member built into the core or wound around the outside of the array cable. Strength members are often made using synthetic fibers such as Kevlar or Arimid substitutes that are lightweight, flexible, and extremely strong. They can be centrally located inside the cable or they can be woven around the conductors using specialized assembly spooling machines. Manufacturers such as Cortland Cable Company, Yale Cordage, Falmat Cable, National Wire, and others specialize in the manufacture of custom oceanographic array cables. Important to the basic array design is the decision to use a flooded or sealed cable. Flooded cables are those in which the conductors themselves are made with a polyurethane or comparable outer jacket and are completely sealed against seawater incursion. The conductors are wound together, possibly in conjunction with a strength member, and then typically encased in a polyester woven abrasion cover. This outer cover floods and exposes all of the conductors to seawater. Installation of hydrophone elements with this type of cable requires each conductor to be properly sealed at each hydrophone location. Alternatively, cables can be made with an extruded polyurethane outer jacket that encases the entire array cable and is completely sealed. Typically a "water block" agent is used to fill the air voids within the cable and prevent water from migrating inside the cable should a leak occur. This construction allows for the hydrophone element to be molded onto the outer cable jacket creating a seal. The water blocking compound can hinder wire breakouts as it must be removed, but can be worked with. For vertical line arrays, a fairing is required to prevent vortex-induced strumming when suspended within the water column subject to current. The fairing designs vary from one company to the next and can range from fiber hairs a few inches in length

woven onto the cable to molded ribbing on the cable jacket, both intended to disrupt the flow around the cable and prevent vortex creation on the low pressure backside. The selection of conductor type for data telemetry is largely driven by bandwidth requirements and length. As mentioned previously, twisted pair wires result in a smaller cable, but cannot support MHz signals over distances in excess of 100 meters without incurring losses. While this may be fine for many scenarios, coaxial cable may be required for high frequency signals or for long distance signaling. Fiber optics are useful for fixed installations but introduce termination and splicing complications, additional power consumption, higher costs, and longer construction times for line array prototype systems with 100s of elements.

2.10.2 Conformal Coating

Printed circuit boards require pre-treatment with a conformal coating prior to encapsulation with urethane. A conformal coating is a compound that is applied as a liquid with very low viscosity. Exposure to oxygen starts the curing process. The coating penetrates underneath components on the PCB and can be applied inside larger components with plastic cases containing air voids, such as large DC-DC switching supplies. Without this conformal coating, the urethane would not be able to fill the air voids underneath surface mount resistors, for instance, and the circuit would fail due to component cracking under pressure. The urethane can be applied once the conformal coating has fully cured. Preparation of the PCB prior to application of the conformal coating consists of a denatured alcohol wash down and subsequent drying to remove any contaminants, like solder flux, for proper adhesion.

2.10.3 Encapsulating

Urethane encapsulation of hydrophone elements has been standard practice for many years. Most urethanes are made up of two parts, a base polymer and a curing agent. Urethanes vary in color, hardness, curing time, pour viscosity, thermal conductivity, dielectric properties, and hydroscopic properties. Urethanes with acoustic impedances, product of density and bulk sound speed, very close to seawater are readily available. Cytec brand EN1556 is a two part urethane used at ARLUT for decades for hydrophone encapsulation. The urethane can be stored in a sealed container, typically dry Nitrogen back-filled, but should be placed in a warming oven at 105 degrees farenheight. Warming the urethane helps to dissolve the urethane polymer and decrease its viscosity prior to mixing. It is important to note that the higher the urethane temperature is when mixed, the faster the cure time is. Care must be taken when mixing the two parts to remove trapped air bubbles and avoid introducing moisture. Trapped air is removed by placing the mixed urethane into a vacuum chamber drawn down to 30 inches of mercury for about 5 to 7 minutes. The urethane is then poured into a two part mold clamped around the hydrophone element, which is wired into the array cable directly or may be wired into a connector so that it can be removed. Proper mold design incorporates a pour hole to accept the urethane and a vent to allow air to escape. Curing may be done at room temperature or in a heat box depending on the desired cure time, which is approximately 12 -16 hours for working strength and 24 hours for a full cure.

2.10.4 Pressure Testing

As many individual components as possible should be tested leading up to finalization of a prototype design. This requires access to a pressure vessel large enough to accommodate the components and if need be a small prototyping circuit board that can be used to solder the components to for in-situ testing. Non-conducting oil, such as

castor or mineral, can be used inside the pressure vessel which allows for testing with applied electrical power if an electrical pressure rated feed-through is present. Section 4.6 describes in detail the pressure vessel setup used during the prototype development for this thesis. Once a complete prototype element PCB has been designed, fabricated, bench tested, and encapsulated, a 60.6 MPa test corresponding to a 6,000 meter depth can be performed to validate the completed design, including verification of the conformal coating and urethane encapsulation process. There are a number of commercial facilities around the United States that offer contract access to large pressure vessels with more than adequate electrical feed-through options, laboratory power supplies, and test and measurement instrumentation. Fortunately for this project, all testing was performed in-house using ARLUT equipment and pressure vessels.

CHAPTER 3 PROTOTYPE ARRAY DEVELOPMENT

3.1 DIGITAL TELEMETRY ARRAY HYDROPHONE NODE

Each hydrophone element and corresponding array interface PCB can be referred to as a node. For the purpose of this thesis, they will be referred to as DTA Nodes, short for digital telemetry array nodes. The design and fabrication of the DTA Node represents the bulk of the work as it accounts for the hydrophone selection, amplifier design, A/D converter selection, local processor selection, transceiver selection, and step-down power conversion, all of which must be pressure tolerant. The DTA Node will drive the overall system's acoustic performance, bandwidth limitations, and element spacing options. Power consumption for the entire DTA Node must not exceed ¾ of a watt. Figure 3.1 calls for development kits to be used prior to fabrication of the first prototype. This allows the designer to experiment with various sections of the design fairly quickly in order to identify any required changes in the design concept prior to investing time and money into a custom PCB layout. The following prototype hardware description sections are broken down, similar to previous chapters, into primary functional areas.

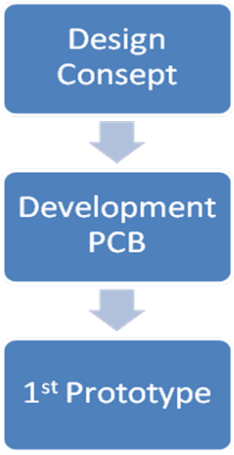

Figure 3.1: DTA Node design process

Before the design could be broken up into separable areas, a general concept covering the entire DTA Node PCB was needed. Figure 3.2 depicts the basic sensor node functional block diagram.

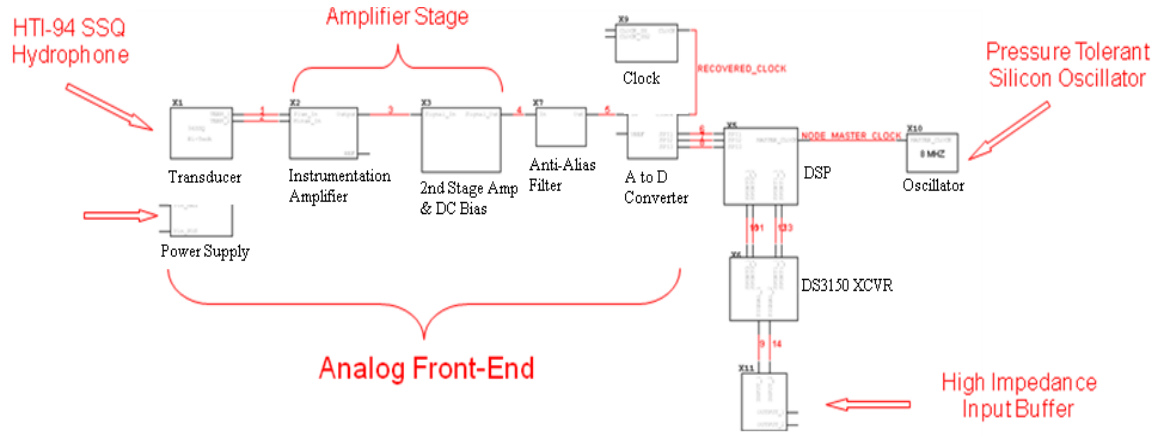

Figure 3.2: DTA Node initial design concept diagram

3.1.1 Analog Front End

The acoustic performance of the array is, after all, the defining characteristic relative to the data products it generates. To restate the objectives, this array design is intended for deep ocean surveys requiring good sensitivity, low self noise, and adequate dynamic range. As part of a line array, each element should be omnidirectional and have a flat frequency response from 10Hz to 4 kHz. From Figure 2.4, the average deep ocean ambient noise level in Sea State 0 is 45dB re 1µPa at 1 kHz and decreases with increasing frequency. A 16 bit A/D convertor will provide 90dB of dynamic range, given that the hydrophone signals are bipolar, resulting in a 6dB reduction in the peak-to-minimum level that can be sampled. The analog front end design, therefore, needs to map the hydrophone output from 45-135dB acoustic input levels into the A/D converters input range. There are three primary variables that can be leveraged in order to tailor the front

end design: hydrophone sensitivity, amplifier gain, and total self noise. All three of these factors are inter-related. Both hydrophone and amplifier self noise are discussed in section 2.1.4. A High Tech HTI-94-SSQ model hydrophone, shown in Figure 3.3, was selected for this prototype. The cylindrical air-backed un-amplified hydrophone has a sensitivity of -195 dB re 1V/µPa, is rated to full ocean depth, has a flat frequency response from 10Hz to 5 kHz, has a free capacitance of 3.5 nf, and has approximately 1" tall x 1" diameter dimensions.

Figure 3.3: HTI-94-SSQ Hydrophone

Given that C_f = 3.3e-9, Δf = 4 kHz, $\tan\delta$ = .005,

from,

$$R_h = \text{Real}\{1/j\omega C_f (1 - j\tan\delta)\} = (\tan\delta/\omega C_f)/(1+\tan^2\delta) \approx \tan\delta/\omega C_f, \tan\delta << 1 \quad (3\text{-}1)$$

and,

$$10\log_{10}\left\langle p_n^2 \right\rangle = -198\text{dB} + 10\log_{10} R_h - 20\log_{10} M + 10\log_{10}\Delta f \quad (3\text{-}2)$$

the hydrophone self noise curve can be plotted as shown in Figure 3.4. Clearly, the hydrophone self noise is shown to be around 41 dB at 10Hz and decreases with frequency. The analog devices AD627 instrumentation amplifier was chosen for the 1st

stage of the DTA Node amplifier circuit. The AD627 has high common mode rejection, high input impedance, variable gain up to 60 dB, and 38nV/root Hz @ 1 kHz at the 40 dB gain setting per manufacturer's data sheet. We can convert the amplifier input referred self noise to an equivalent noise pressure level spectral density using the hydrophone sensitivity. Figure 3.4 shows the calculated, equivalent pressure, self noise spectral density for both the front end amplifier 1st stage and the DTA node hydrophone plotted against a typical SS0 ambient noise curve published by Wenz.

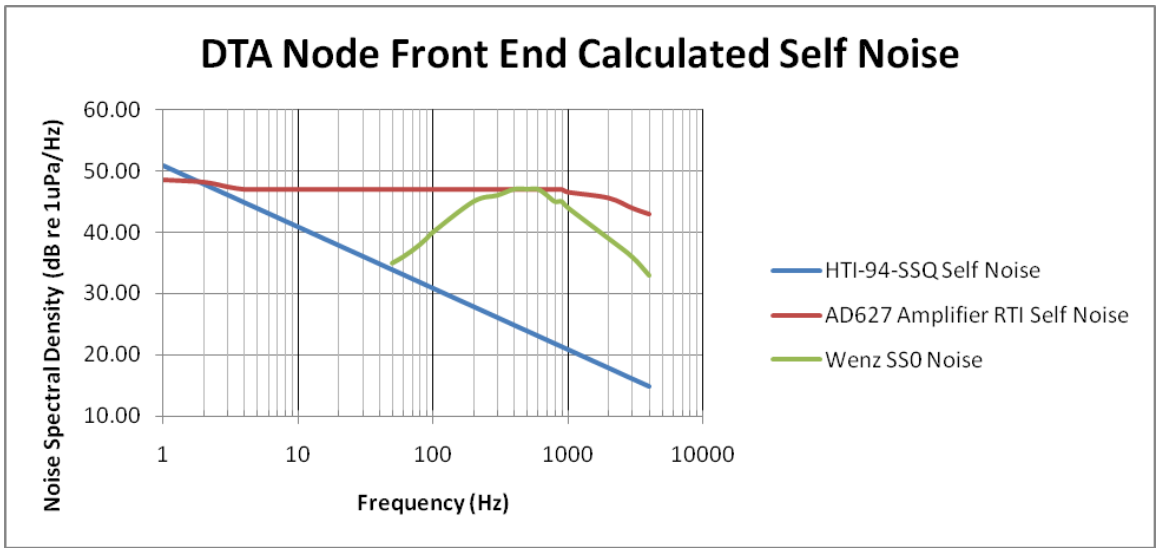

Figure 3.4: DTA node front end calculated self noise

Uncorrelated noise may be added using the square root of the sum of the squares of each individual contribution. It can be seen from Figure 3.4 that while the hydrophone has excellent self noise characteristics, the overall design will be limited primarily by the amplifier, which for most of the operational band has a noise level above the SS0 ambient noise level. Future design revisions should employ a lower noise 1st stage amplifier to improve performance under quiet conditions. The DTA node front end design incorporates two additional operational amplifiers from an LM8272 IC. The first op-amp

achieves an added 37 dB of gain with a 2.5 volt DC bias in order to move the bipolar hydrophone signal into the middle of the A/D converters 0-5 volt input range. Since the first op-amp is in the inverting configuration, the second op-amp is used to invert the signal again with unity gain and also incorporates an active 1-pole low pass filter in the feedback circuit to provide anti-alias filtering for the delta-sigma converter. Figure 3.5 shows the front end amplifier schematic.

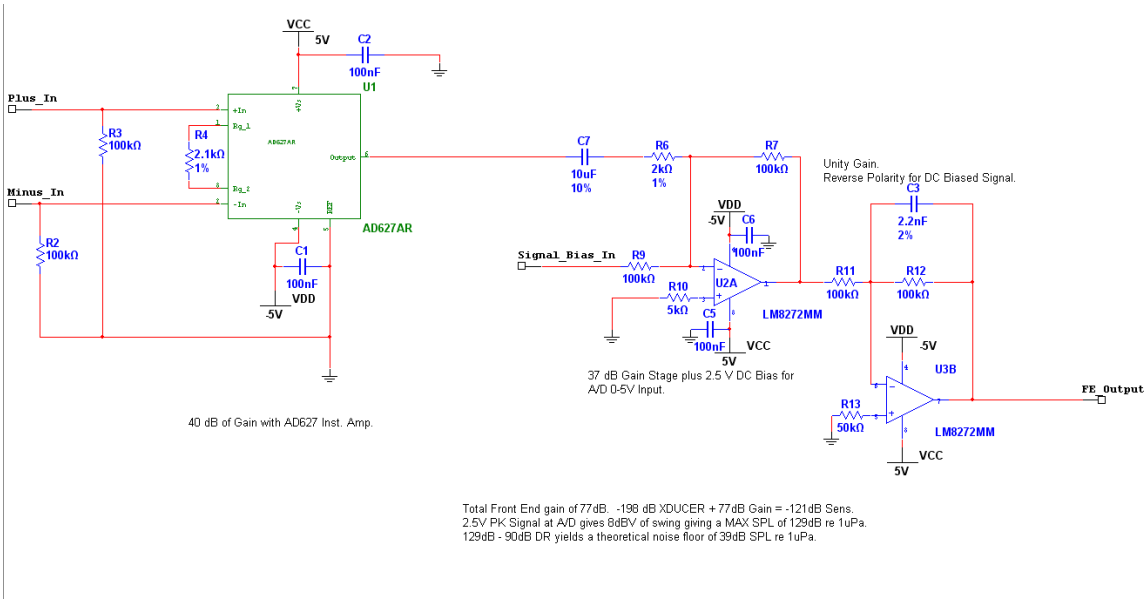

Figure 3.5: DTA Node front end amplifier schematic

The additional amplifier stages will introduce additional noise; however, their influence on the overall noise figure is less pronounced given that they follow a 40 dB gain section.

3.1.2 A/D Converter

A 16 bit single supply, +5V, 4 channel delta-sigma A/D converter was selected for its advantages over traditional A/D converter architectures. The Burr-Brown ADS1174 converter provides a 7mW per channel low power operating mode with sample rates up to 10 kHz. Data is read via an SPI serial interface which can be configured to

multiplex all four channels over the same SPI port. Figure 3.6 shows a schematic of the DTA node A/D configuration.

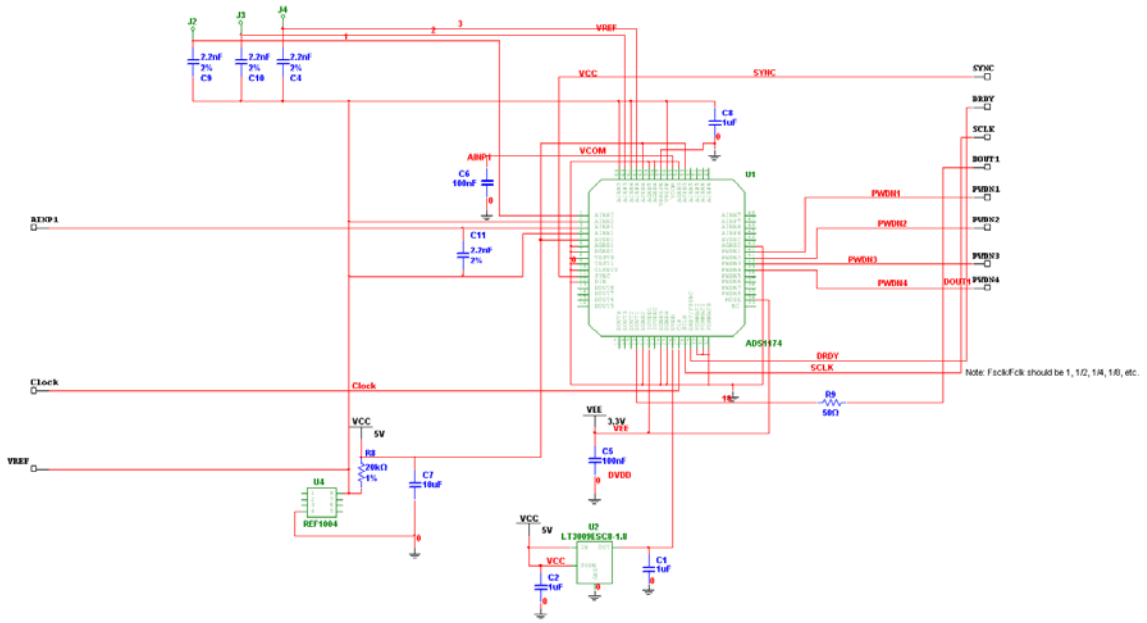

Figure 3.6: DTA Node A/D Schematic

Signal inputs are measured differentially and sampled by the delta-sigma modulator at 64 times the output data rate. The oversampled data then passes through a linear phase digital FIR filter that provides 100 dB of attenuation for signals that lay just outside the passband up to the modulator frequency. A single pole anti-alias filter is still needed to eliminate the possibility of high frequency noise aliasing down.

3.1.3 DSP

Analog Devices ADSP-BF538F digital signal processor (DSP) was used for the local DTA Node processor. The 538F is a fully featured DSP that not only provides the necessary serial interfaces for reading data from the A/D converter and communicating with the array telemetry transceiver, but also offers the flexibility to perform local

element level digital filtering, processing, and custom telemetry protocol implementation. The Blackfin 538F has 512KB of internal flash memory for holding program code without the need for adding external memory to the design and can operate at core clock frequencies up to 533MHz. Power consumption varies according to clock speed, core voltage, and the usage of peripheral interfaces, all of which can be adjusted using integrated application programming interface (API) commands to control an external core voltage regulator and internal clock multiplier. Power consumption figures for this design ranged around 350mW for the DSP itself.

3.1.4 Transceiver

Implementation of the DS3 43MHz signaling over coaxial cable or short run twisted pair wiring requires the use of a DS3 line interface transceiver. The Dallas Semiconductor DS-3150 performs all of the functions required to drive data, provide received clock and data recovery, loss-of-signal monitoring, jitter attenuation, and local processor communication over a SPORT interface with close to 200mW power consumption at 3.3V. The transceiver is designed to drive a 75 ohm transmission line through a 2:1 step down transformer and receive signals through a 1:2 step up transformer. For short range signaling, the transceiver is not greatly affected by impedance mismatch in the transmission line, as discussed later in section 4.5. When used with 75 ohm coaxial cable, the transceiver can achieve very good signaling over cables up to 375 meters long. While designed for 43 MHz standard signaling, the transceiver can be operated at lower frequencies provided the master clock sourced to the local transceiver matches the transmit clock frequency and that the remote transceiver is also configured with matching frequency clocks. Given that the transceivers perform

clock recovery via a phase locked loop circuit using the received data signal, the local and remote clocks need not be in phase.

3.1.5 Power Supplies

Array cables of considerable length with large element counts can have amperage draw requirements that must be considered. Higher supply voltages reduce the current required for a given power demand down the array and minimize power losses due to resistance in the array cable itself. When trying to minimize the size and weight of an array, there is only so much a designer can do to increase the wire gauge of the conductors and lower the impedance. While high voltage insulated wiring is available, as well as corresponding power converters, 18-72 volt input range DC-DC switching power supplies manufactured by Calex Inc. were used in this prototype. These converters have proven to be very reliable, efficient, and easy to use in previous designs. Physically, they are rather large compared to other switching supply designs available in a single IC. It is not as common, however, to find a switching supply that can convert 72 volts down to 3.3V with good efficiency in small packages, though they do exist. For proof of concept, the Calex 48S3R3.700SMT and 48D5.500SMT provided the necessary off the shelf performance in a package type that was found to be pressure tolerant as discussed later in section 4.6. Switching regulators offer efficiencies up to 85% in most designs and are more efficient when operated near maximum output current and when the difference between input and output voltages are the least. Linear regulators are usually much less efficient, as they are simply dissipating energy to achieve the desired regulated voltage. Using a switching regulator at each DTA node allows a higher voltage supplied down the array cable to be converted locally at each element. Proper fusing at each node can help provide some immunity to a single node failure shorting out the entire bus.

3.1.6 Prototype Node Version 1

Chapter 4 discusses the hardware test configurations and results all the way from development kits to custom prototype hardware developed for this project. To avoid repeating material, this section focuses on the development of the actual prototype itself. The first step in moving from development kits to an operational prototype was to design custom PCB incorporating the various hardware elements discussed previously. PCB designs incorporating DSPs and high speed serial data lines must be attempted with care to avoid layout flaws that can render the design in-operable due to improper routing of traces or improper trace impedances. High speed signaling in the 10's of megahertz requires treatment of traces like transmission lines. The PCB layer thickness, trace width, length, and termination impedance are important in preserving the signals. There are numerous design tools available to assist in proper trace layout.

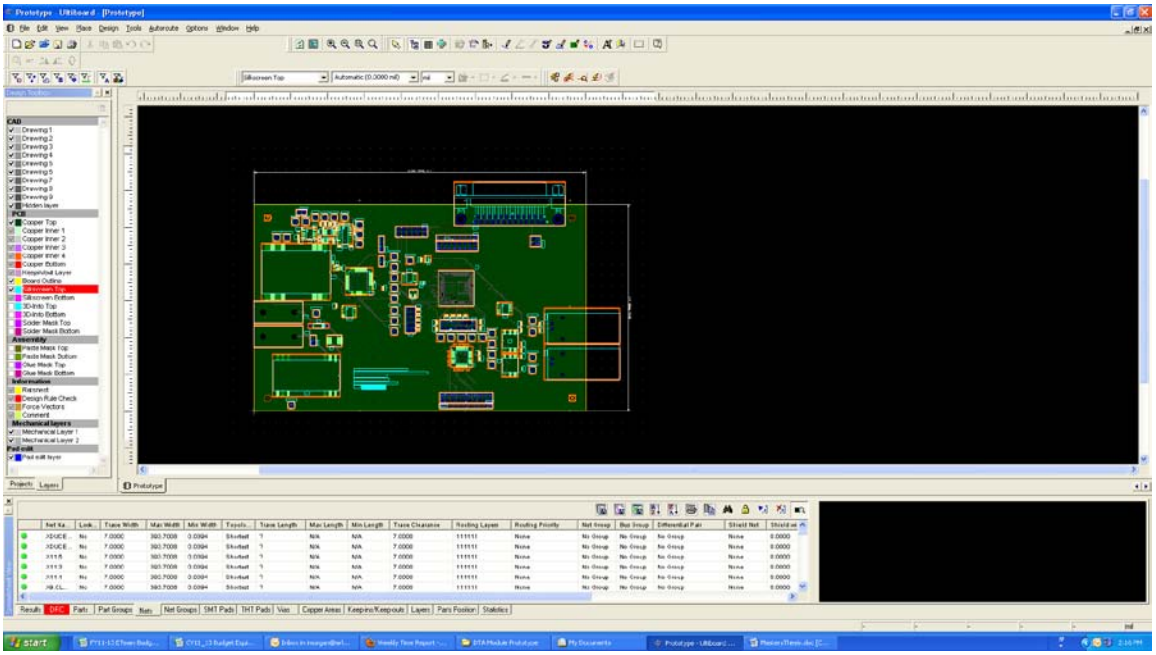

Figure 3.7: Screenshot from National Instruments Circuit Design Suite 10, Ultiboard Layout

Rather than designing for a final form-factor, a less stringent design was chosen using more board space in order to obtain some confidence in the design approach. National Instruments Circuit Design Suite version 10 was used for the schematic capture, Multisim, and the board layout, Ultiboard. Figure 3.7 shows a screenshot from the Ultiboard layout program. The complete circuit can be designed in Multisim; component package types associated with each part, and then import the design into Ultiboard for layout, similar to other commercially available design tools. The first manufactured prototype can be seen in Figure 3.8 below.

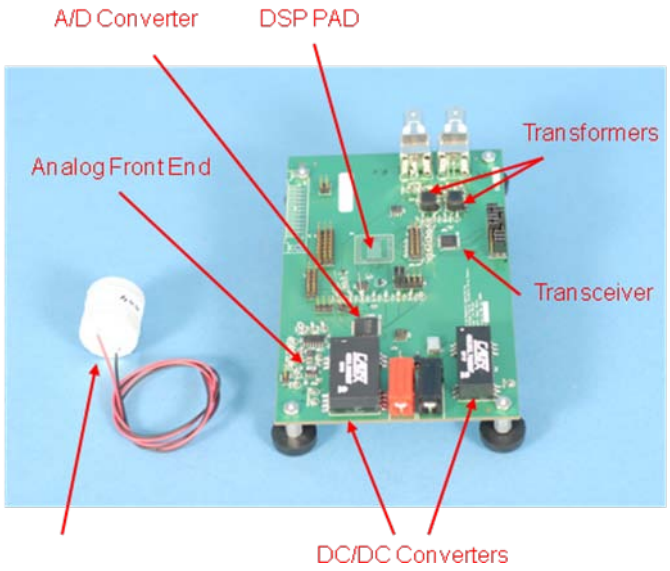

Figure 3.8: Custom DTA Node prototype version 1.0

Eagle Circuits in Dallas, Texas manufactured the first prototype PCB and unfortunately there was a flaw in their fabrication of the DSP pads. The BlackFin DSP's package type is a 316 pin mini ball grid array (BGA). This type of chip requires very small pads on the board. Underneath each tiny contact is a small ball of solder that adheres to the pad when wave soldered. Our design required small vias, thru-hole connections between layers in the board, to be placed inside the pads. When soldered,

the via holes pulled all of the solder away from the contact and in some cases there was too little solder remaining to make good contact. The manufacturer attempted to re-solder the DSPs with no success and delivered the boards without the DSPs installed. Fortunately, all other portions of the board were functional allowing the power supplies, front end amplifier, A/D converter, and the transceiver to be tested as built. The BlackFin DSP from our development kit was then wired into the prototype board to complete the testing.

3.1.7 Prototype Node Version 2

The first prototype identified a potential risk in the manufacturing process for the DSP pads. Prior to manufacture of the second prototype, we consulted with a few different vendors about steps that could be taken to prevent the same problem. Additional solder can be flowed into the vias prior to component placement for low production run board designs like this eliminating the liability. Future layouts can move the vias away from the pads by more time consuming trace routing in order to eliminate the conflict all together. Testing of the first prototype had yielded an otherwise successful design. Reconfiguration to improve the form factor and incorporate a slot for the hydrophone in the PCB shape was the next design goal. A block diagram containing the primary node components in a logical layout relative to data flow, as well as, a slimmer shape to compliment attachment to the array cable lengthwise is shown in Figure 3.9. Care was taken to minimize high frequency trace lengths and to physically separate analog from digital signal traces to minimize noise. The board layout was re-worked within Ultiboard. The final board layout was a 6 layer board approximately 2 inches wide by 5 ¾ inches long. A screen capture of the board layout is shown in Figure 3.10. The hydrophone cutout allows for attachment of the hydrophone using a flexible urethane

adhesive. Additional space was left open on the top and bottom side of the PCB for future addition of analog front end amplifier components to support the 3 available A/D converter channels that are not being used in this prototype single hydrophone design.

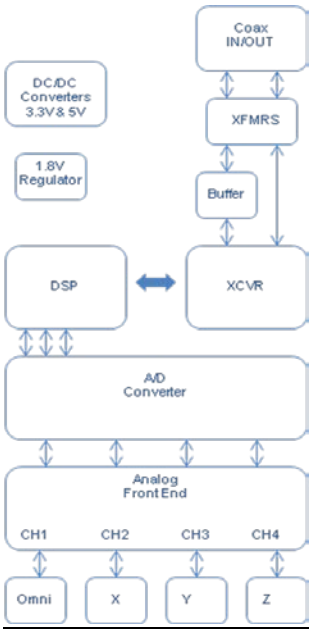

Figure 3.9: DTA Node prototype version 2.0 block diagram

The DSP is programmed through the JTAG header located on the top side of the board. In order to allow for future programming changes to the DTA node, a wet pluggable Subconn connector, shown in Figure 3.12, will be potted into the element. A dummy plug will be used to seal off the connector when deployed. JTAG hardware can be sensitive to added cable lengths due to signal degradation. The wet pluggable connectors incorporate non-standard cable wiring for JTAG applications. The cable length was kept to a minimum and the setup tested successfully.

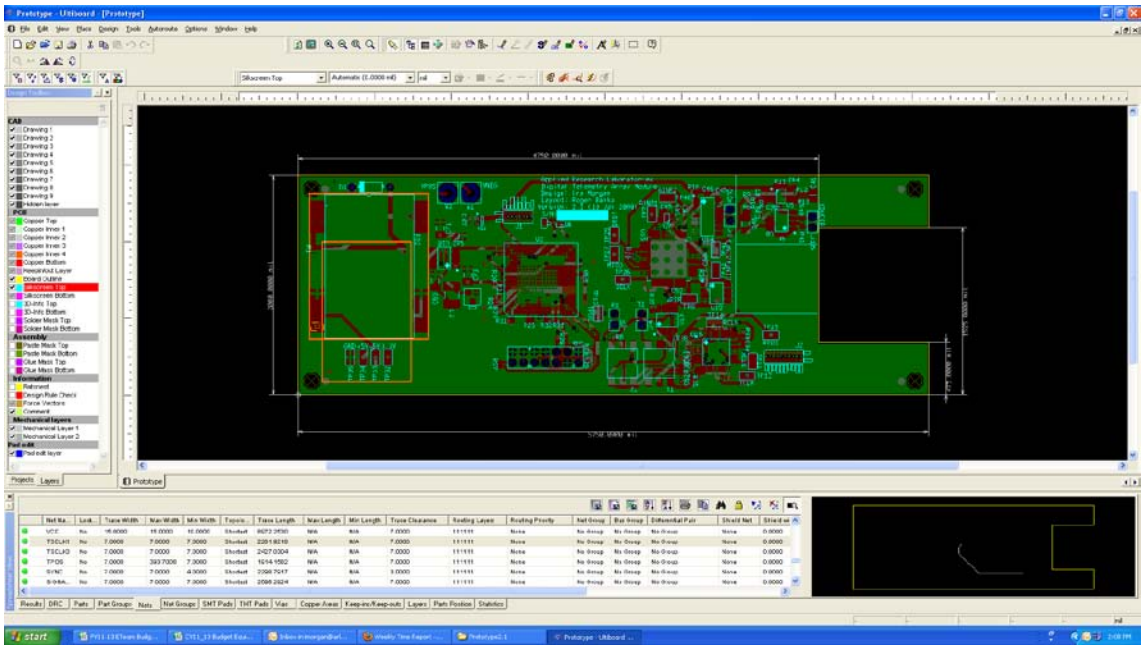

Figure 3.10: DTA Node prototype version 2.0 Ultiboard PCB layout

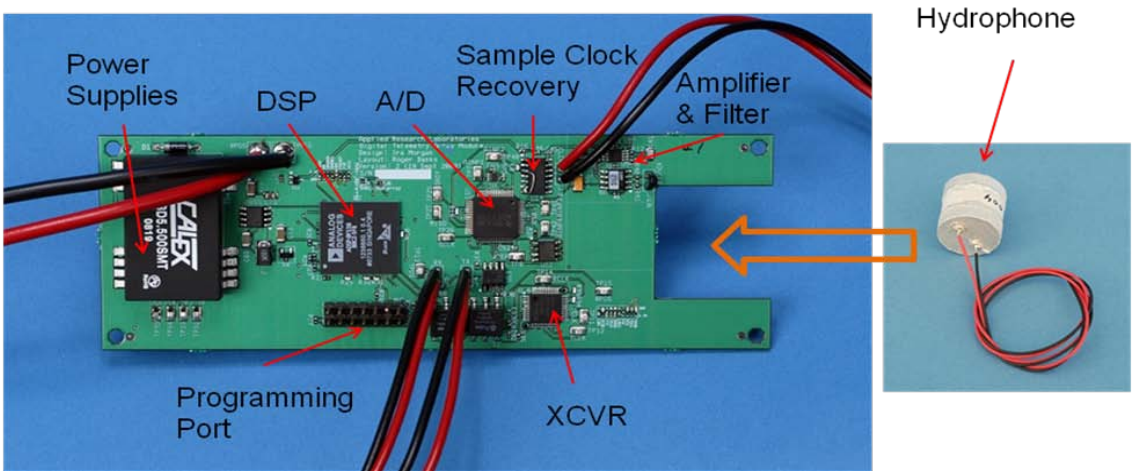

Figure 3.11: DTA Node prototype version 2.0 fabricated custom PCB

A second underwater connector provides the power, clock, and data interface. Utilizing connectors, rather than hard wiring the prototype, allows substitution of test cables for the array cable when needed.

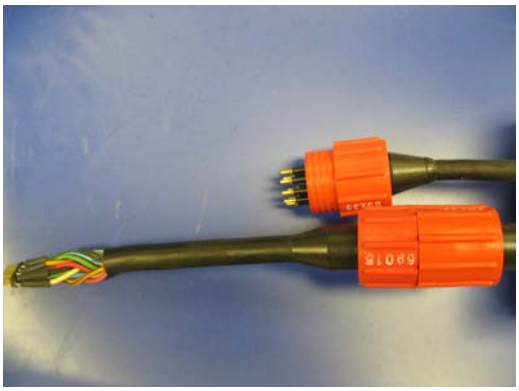

Figure 3.12: Underwater, wet-pluggable, JTAG DSP programming connector

3.2 URETHANE ENCAPSULATION

Immersion in salt water requires proper encapsulation of the DTA node to prevent water incursion onto the PCB or the hydrophone element. Two part polyurethane potting compounds provide excellent water proofing, abrasion resistance, and acoustic properties. For low power designs such as this, thermal conductivity is not an issue. Temperatures at the sea floor in deep ocean environments are often around 3 degrees Celsius. This will cause many urethane mixes to harden, which can affect some sensor designs, but they often retain their elastic capability relative to non-acoustic flexure. Pressure tolerant encapsulation requires an additional step beyond the typical denatured alcohol wash-down. Conformal coating of all electronic components with an extremely low viscosity agent is vitally important, as discussed in section 2.10.2. For this prototype, Parfix™ brand cyanoacrylate adhesive, essentially a low viscosity Super Glue®, was selected for the conformal coating. The adhesive is applied to each and every surface mount component including resistors. There can be no air gaps remaining inside or beneath any components. For larger components, like the DSP, a small "dam" was created around the IC using a small bead of hot glue. This allows the adhesive to build up underneath the IC without running out. The Calex power supplies have a large outer plastic case with the

switching regulator electronics inside. Previous testing was done with the internal electronics in oil to verify pressure tolerance. In order to eliminate the air inside the power supply, the case needs to be filled with a suitable conformal coating. Given that the switching power supplies are the most likely components to generate heat, a low viscosity, relatively high thermal conductivity epoxy was used instead of the adhesive.

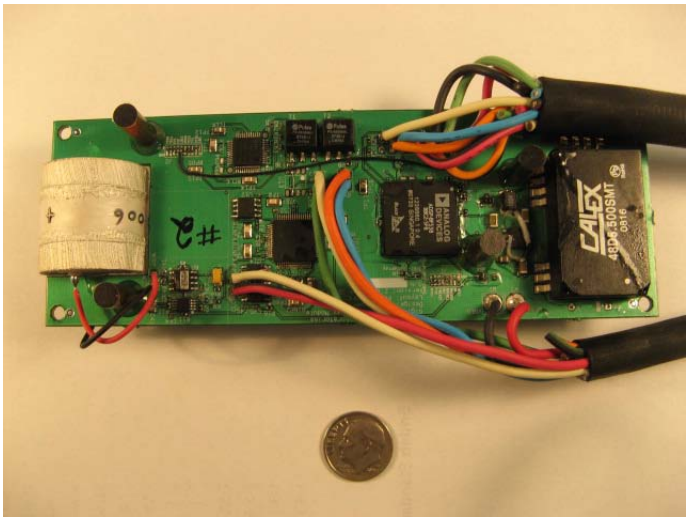

Figure 3.13: Top View, DTA Node prepped for urethane potting

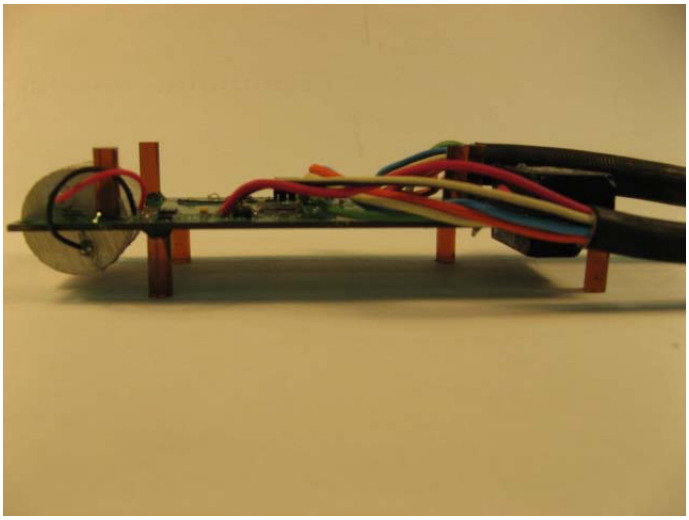

Figure 3.14: Side View, DTA Node prepped for urethane potting

Two opposite corners of the Calex supply cases were opened for fill and vent holes. Figure 3.13 and Figure 3.14 above show the DTA node prototype after conformal coating and epoxy have been applied. Small urethane cylindrical spacers were made and attached with two part 5 minute epoxy above and below the PCB to locate it in the center of the mold.

Figure 3.15: DTA Node inside the urethane potting mold

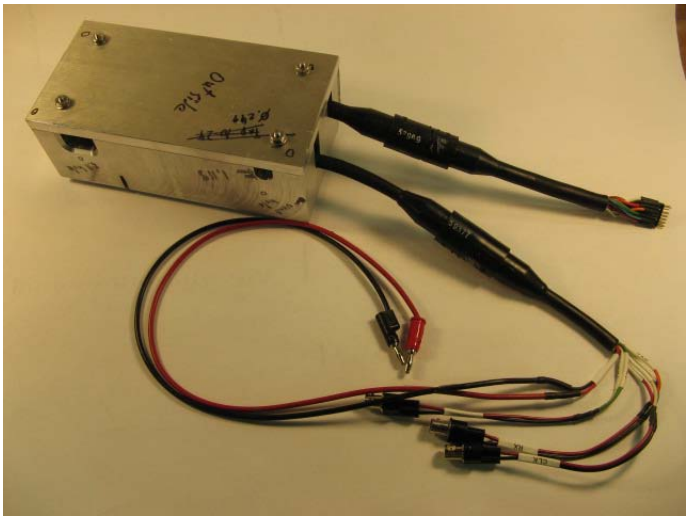

Figure 3.16: DTA Node enclosed inside the urethane potting mold with JTAG & Array Test Cables

A simple rectangular potting mold was machined out of aluminum. The mold consists of alignment pins for seating the lid, urethane pour and air vent holes, cutouts for the electrical connectors, and a few threaded holes in the bottom for pushing the part out of the mold after curing. Moldable duct seal is used to seal any gaps in the connector cutouts to prevent urethane from leaking out.

3.3 Array Cable

A 153 meter long off the shelf full ocean depth rated ROV video cable from McCartney Offshore was purchased to serve as the prototype array cable. The cable contains two 75 ohm coaxial cables, four twisted pairs, and one quad. A polyurethane outer jacket allows for very good urethane adhesion.

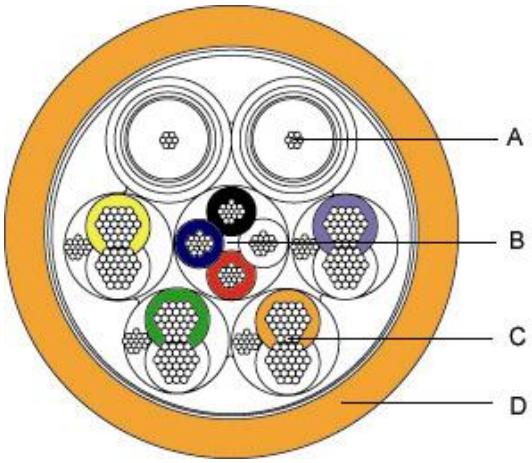

Figure 3.17: DTA Node prototype array cable. McCartney Offshore 6120 ROV Video Cable

Given the desire to test the telemetry with coaxial cables, should large element spacing be desired, this type of cable was ideal. The two coaxial cables were used for the data telemetry while two of the twisted pairs were used for the power and acoustic sample clock. Analysis of the cable characteristics at pressure are provided in section 4.6

3.4 ARRAY INTERFACE

The array interface was modeled after the DTA nodes themselves. High speed serial I/O between a local processor and a matching transceiver are required for compatibility with the array telemetry. The same BlackFin DSP and Dallas Semiconductor DS-3150 transceiver make up the core components of the array interface. The BlackFin and DS-3150 development kits were wired together, as shown in Figure 3.18, to make-up the interface eliminating the need for custom hardware at this stage.

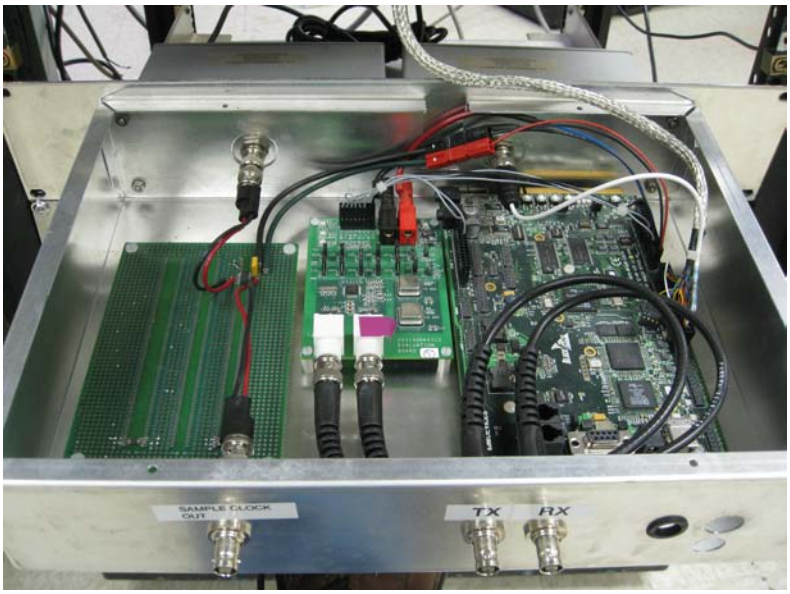

Figure 3.18: Array Interface Module (AIM)

The LabVIEW programming software, via NI-DAQmx, already contains drivers for reading and writing data over a parallel I/O port. The same can be said for the DSP using Analog Devices' VisualDSP++ IDE and standard API function calls. The parallel I/O interface doesn't require an understanding of communications protocols that might be necessary with Ethernet or USB. A simple command and data packet format can be chosen to accommodate the necessary operational functions of the array. A National Instruments PXI-6534 Digital I/O board operating in a burst handshaking mode with the

DSP worked well with a 10MHz transfer clock. The transfer clock was sourced externally via an Agilent 33220A signal generator due to loading issues when using the built in 6534 clock connected directly to the DSP. A high speed buffer would otherwise have been needed to avoid an external clock.

3.5 Recorder Development

Leveraging existing ARLUT hardware was the goal for recorder development. Most of the Deep Ocean and shallow water recording systems within the Environmental Sciences Laboratory have been upgraded recently and currently use National Instruments PXI form factor chassis, CPUs, A/D boards, and peripheral communications interface boards. These systems are programmed using the LabVIEW programming language and are controlled remotely over an acoustic modem link to the surface ship.

Figure 3.19: DTA array recorder National Instruments bench test hardware

Figure 3.19 shows a 4 channel PXI recorder chassis connected directly to a shipside control laptop via a straight RS-232 serial cable in place of an acoustic modem link. Figure 3.20 below shows the finished prototype recorder, power supply, and array interface rack mounted. Refer to Appendix B for details on the overall system

interconnect diagram, data flow logic diagram, AIM to PXI recorder wiring diagram, as well as parallel I/O timing diagrams.

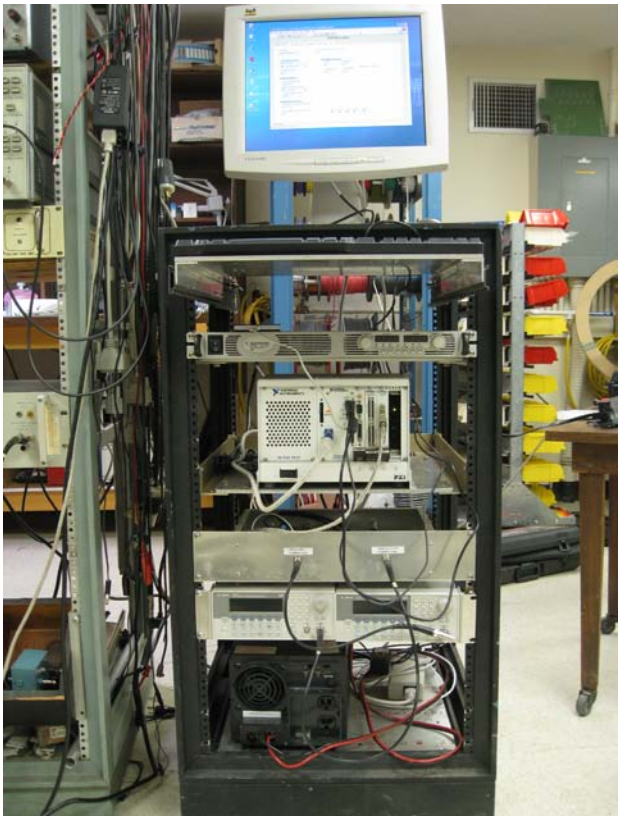

Figure 3.20: Rack mounted DTA recorder, power supply, and array interface

CHAPTER 4 HARDWARE TESTING AND EXPERIMENTAL RESULTS

This section describes the hardware testing of each array component from beginning concept to final design. An acoustic model must be constructed to validate the prototype element node design and hydrophone selection. The front end amplifier's frequency response must be characterized for gain confirmation. The A/D converter operation and interface with the DSP must be verified. The telemetry transceiver performance must be analyzed thoroughly under various cable lengths and incorporating element node connectors which will introduce a change in impedance at the transceivers. The special non-standard IC components must be individually pressure tested to confirm pressure tolerance leading up to a final pressure test of the completed prototype element. Finally, the completed encapsulated element node must undergo an in-water acoustic checkout with data collected via the array telemetry link.

4.1 ANALOG FRONT END TESTING

4.1.1 Amplifier

Using the first custom prototype PCB shown in Figure 3.8, in conjunction with an HP-3562A Spectrum Analyzer, the amplifier's frequency response was measured. The 3562A analyzer contains a built in signal source that can be configured for linear swept sinusoidal output. The signal quality is very low noise and makes for a great analysis tool when used with the 2-channel frequency response measurement mode setting. The source amplitude is limited to a minimum output voltage of 10mV peak. For an amplifier with 77 dB of gain, the amplifier output will peak at $7079 * 0.01 \approx 70V$ which would cause the amplifier output to clip at the 5V rail. Therefore, it was necessary to use at least 25 dB of attenuation on the signal source. The importance of a clean source is even

more important when reducing the signal even further. The spectrum analyzer was configured to sweep from 1 Hz up to 5 kHz. The data shown in Figure 4.1 was transferred directly from the analyzer and is on a dB vs. Log scale. The x-axis units are in Fourier transform frequency bins.

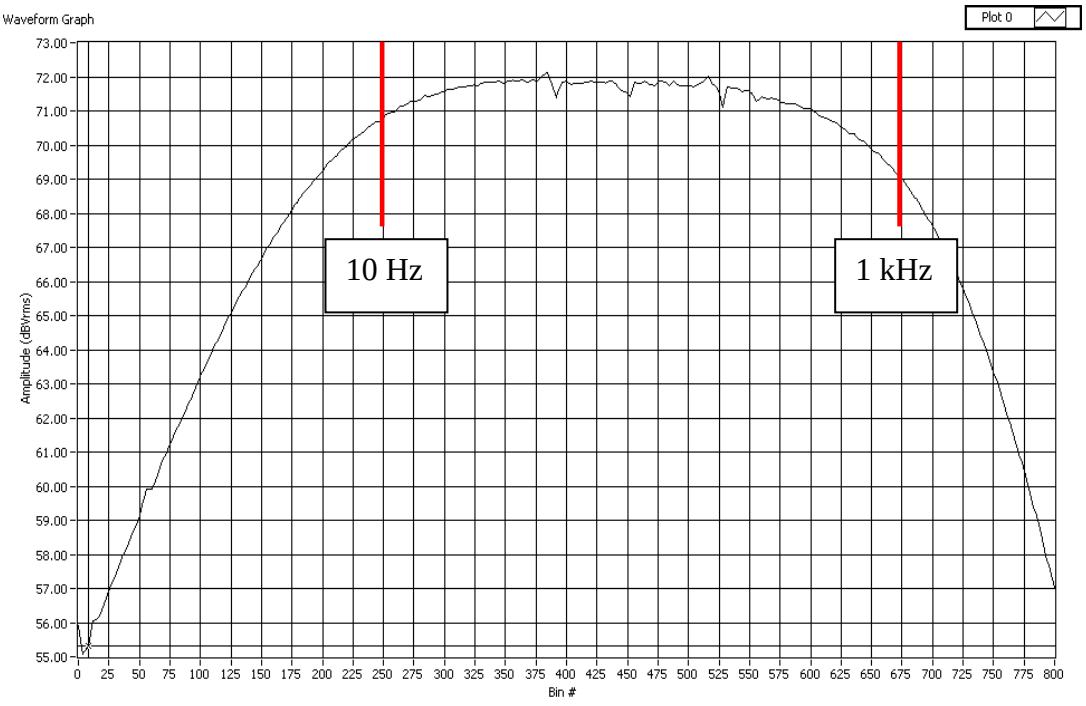

Figure 4.1: DTA Node amplifier frequency response, 1Hz – 5 kHz, with 6 dB passive low pass filter installed.

A single pole passive low pass filter was originally installed between the AD-627 instrumentation amplifier and the LM-8272 Op-amp first stage. A passive RC filter will result in 6 dB of signal attenuation for all frequencies due to the voltage drop across the split resistance, which is evident in the 5-6 dB gain variation from the quoted 77dB. The final front end amplifier design has the passive filter removed, restoring the correct gain. The frequency response of the AD-627 rolls off so quickly beyond 1 kHz, for a gain

setting of 40dB, that a passive filter was simply not necessary. For operation beyond 1kHz, an alternative amplifier should be used.

4.1.2 Hydrophone

The High Tech Inc. model HTI-94-SSQ hydrophone has a receive sensitivity of -195 dB re 1V/µPa and has a flat frequency response from 10Hz to 5kHz. An acoustic model of the PCB representing the shape and planned hydrophone mounting cutout was constructed as shown in Figure 4.2. The hydrophone was mounted inside the fiberglass board using Hardman Double Bubble Urethane. A Burr-Brown PGA-204 instrumentation amplifier was used to provide gain for interfacing to the data collection system at Applied Research Laboratories' Lake Travis Test Station in Austin, TX.

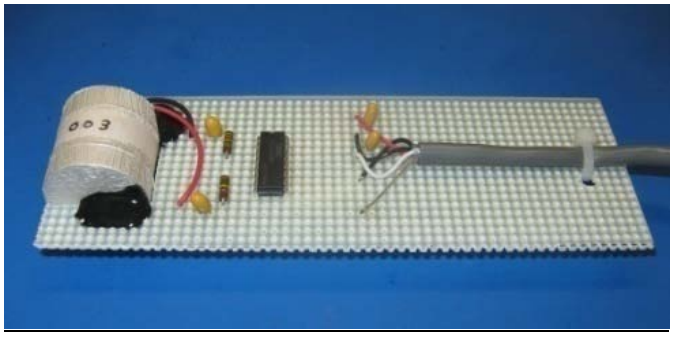

Figure 4.2: DTA node acoustic prototype (HTI-94-SSQ, PGA-204 Amplifier, & submersible cable)

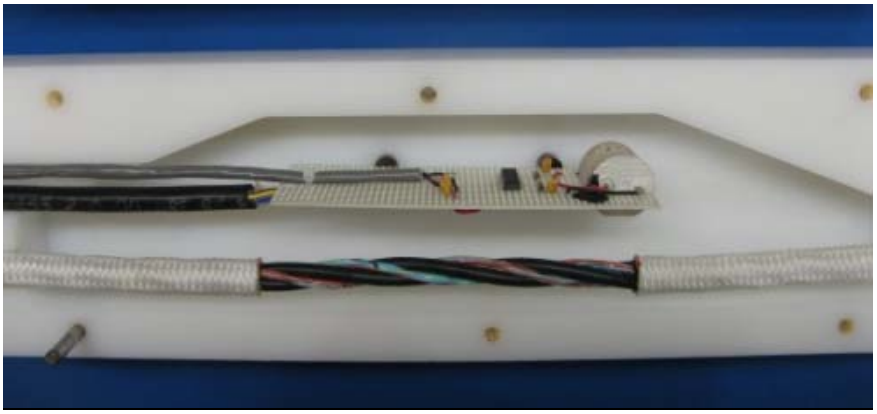

Figure 4.3: DTA node acoustic prototype inside plastic potting mold alongside surrogate array cable

A simple 1 part urethane potting mold was machined out of Delrin with cutouts for the electrical test cable, a sample rubber molded wet pluggable connector, and a second multi-conductor cable to represent the actual array cables potential acoustic affect.

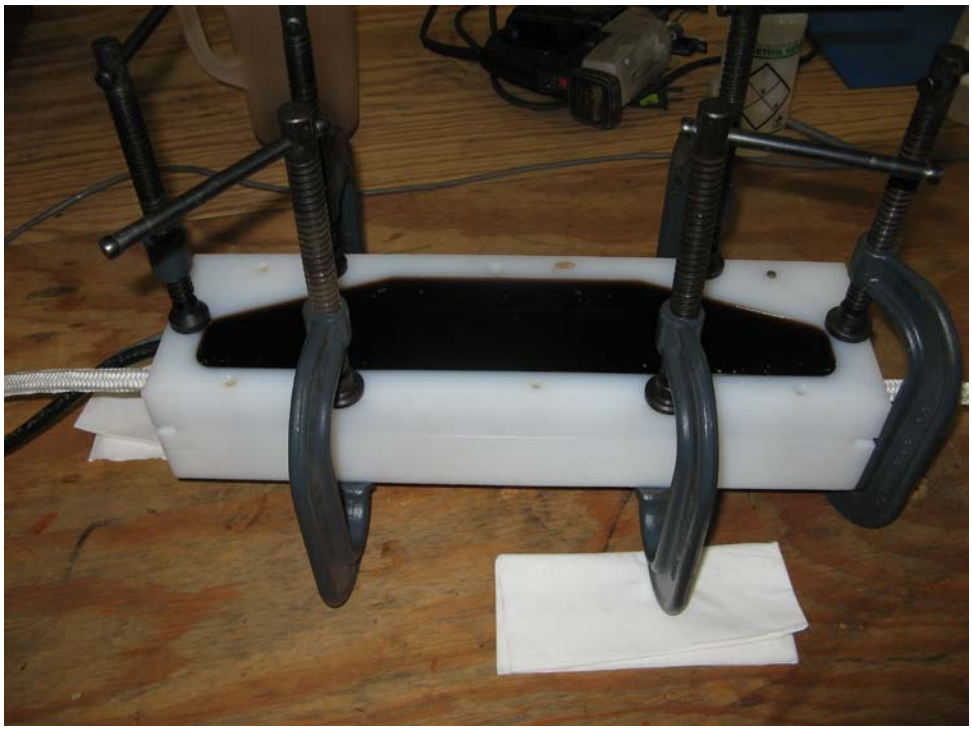

Figure 4.4: DTA node acoustic prototype after urethane potting pour.

The filled mold is shown with the Cytec EN1556 urethane in Figure 4.4 above. Delrin serves as an easy to machine material that the urethane will not stick to, as well as, allowing for removal of the molded part. The finished prototype can now be tested to confirm that the desired omnidirectional directivity has not been compromised. At the Lake Travis Test Station, a NUWC J-9 source and H56 reference hydrophone are used in conjunction with a rotating column and two channel data collection system to measure the directivity pattern in both the vertical and horizontal planes. The source and receivers are placed about 15 feet beneath the surface and 3 feet apart. The small size of the source

(~ 3in. dia.) and the receiving hydrophones allow for the close proximity configuration while remaining in the far-field [1]. Minimizing separation reduces surface reflections and increases signal-to-noise. Figure 4.5 & Figure 4.6 below show the horizontal & vertical omnidirectional directivity patterns respectively at 1kHz for the acoustic prototype. Free-field receive voltage sensitivity measurements were made in ARL's large FIR test tank using a NUWC J-9 source, HTI-90-UD calibrated reference phone, and a National Instruments based USB DAQ. Figure 4.7 shows the calibration results with the amplifier gain removed. The -195 dB re 1V/µPa @ 1m sensitivity was confirmed.

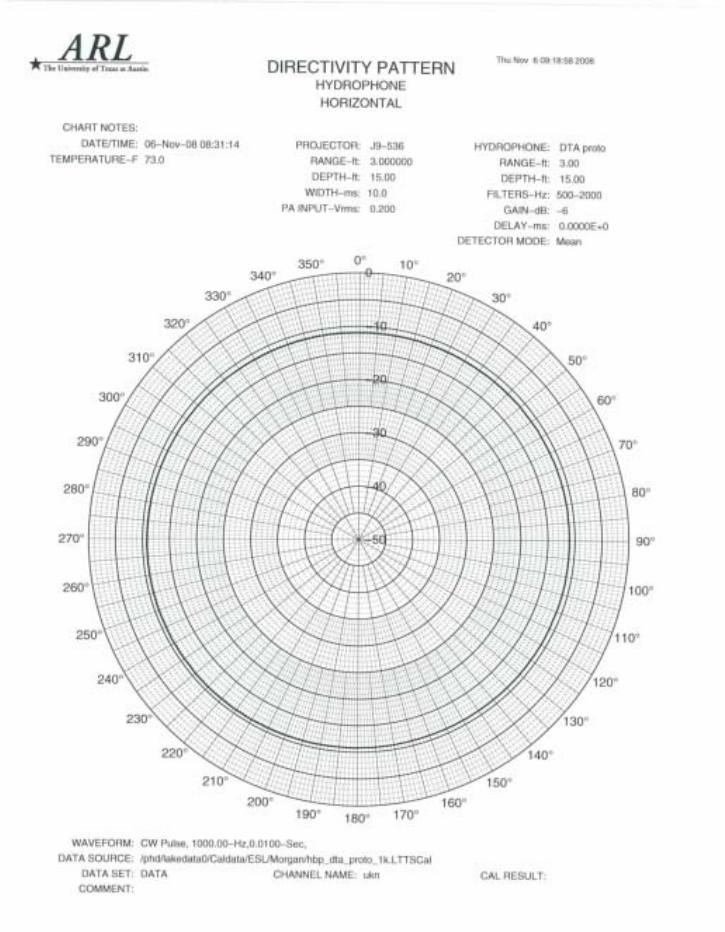

Figure 4.5: DTA node acoustic prototype directivity pattern in the horizontal plane

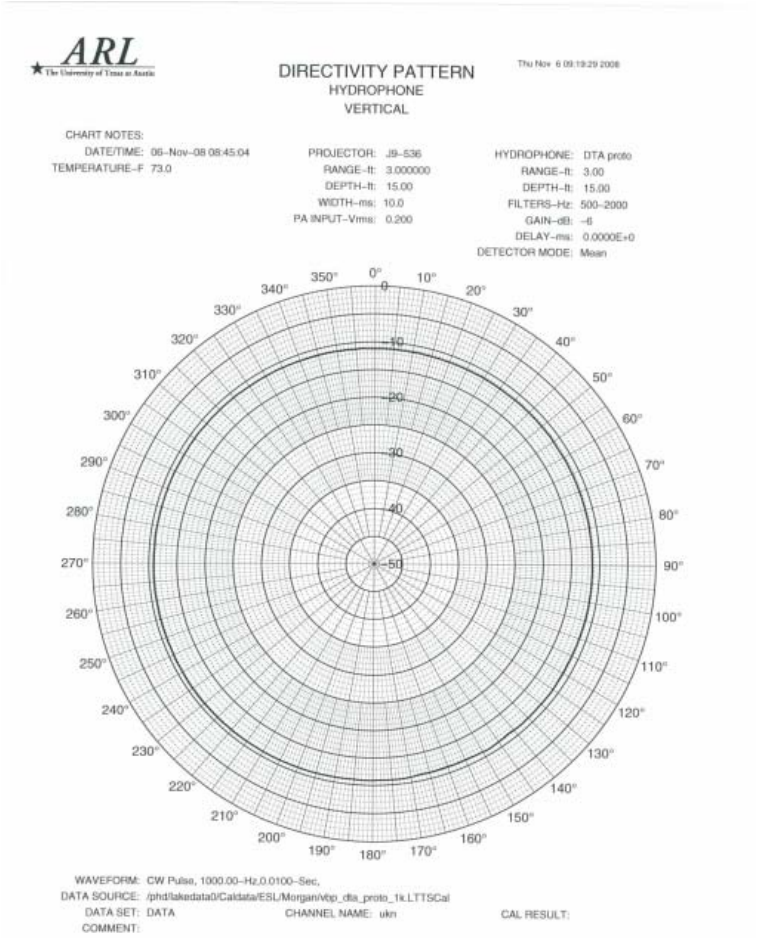

Figure 4.6: DTA node acoustic prototype directivity pattern in the vertical plane

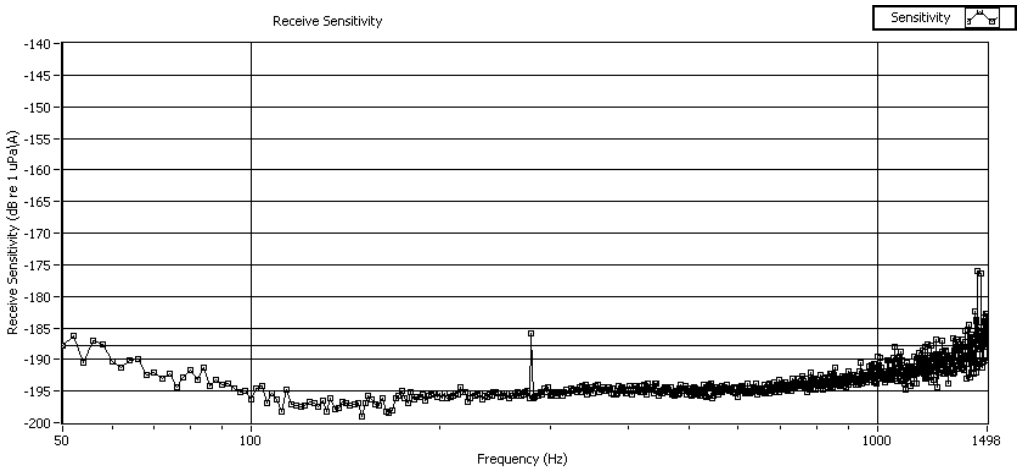

Figure 4.7: Completed DTA node final in-water acoustic calibration plot

Validation of the DTA node design acoustically was an important step prior to moving forward with the actual custom DTA node PCB. Given the positive results with the acoustic prototype, the final custom DTA node was fabricated with the same dimensions. The receive sensitivity frequency response measurement with the final node presented an additional challenge caused by the amplifier design. The single ended section in between the AD-627 and the LM-8272 Op-amps allows 60 Hz noise into the front end and applies the additional 37 dB of gain. This is a common problem when testing in the laboratory and is compounded with such high gain levels. Maintaining a differential signal throughout the amplifier would greatly reduce the influence of 60 Hz electronic interference. For shallow and deep water ocean deployments, the presence of 60 Hz noise is not likely and therefore should pose no problem, however the system must be calibrated and evaluated prior to any at sea deployment. In order to eliminate the 60 Hz interference, the aluminum potting mold was used as a Faraday cage. When the element is placed inside the mold with the lid on and a grounding strap attached, the 60 Hz noise is virtually eliminated.

It might seem that the aluminum mold would make it impossible to perform an accurate calibration. It is certainly true that this method will introduce error into the measurement. Given the low frequencies of interest and the relatively thin mold wall thickness, the impact on acoustic signals is low. Figure 4.8 shows the hydrophone calibration performed in ARL's large FIR test tank. Removal of the mold resulted in 60 Hz noise so great that the signals would clip. Additional steps could be taken to minimize the interference, but were beyond the scope of this thesis.

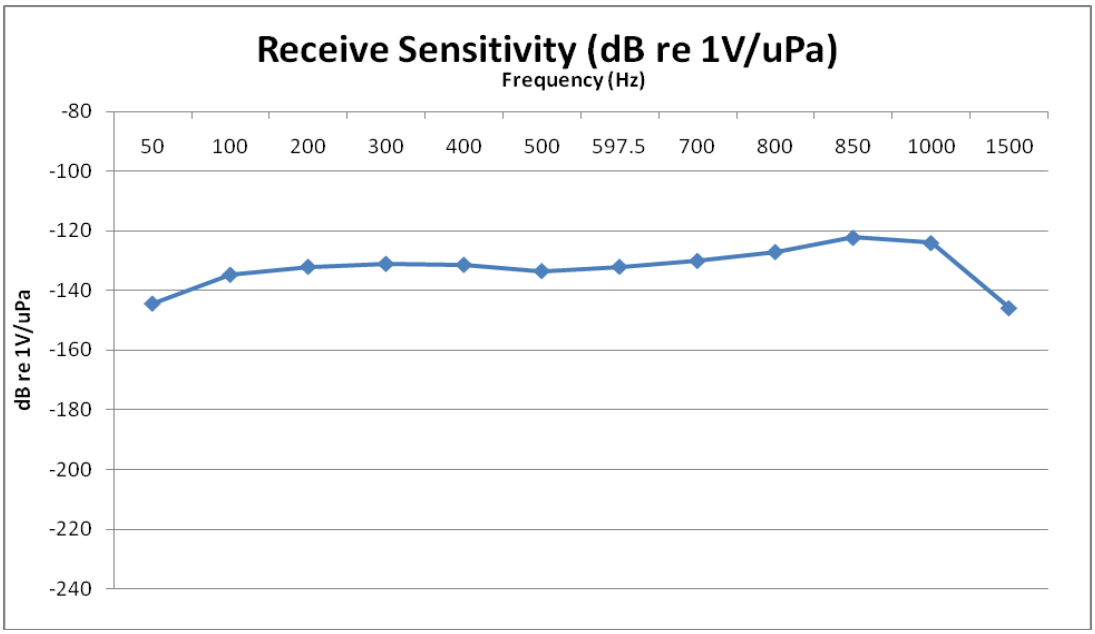

Figure 4.8: DTA node final free-field receive voltage sensitivity with Faraday cage

4.1.3 Analog to Digital Converter

Analog devices VisualDSP++ integrated development environment (IDE) provides a number of debugging and evaluation tools that were useful in testing the A/D since a local processor and SPI interface were required even to read data from the converter. With the final prototype node placed inside the Faraday cage, a 200 Hz tone was generated using a small speaker. A short test program was written for the ADSP-538F DSP that reads data from the converter into a buffer. This transfer is controlled via an interrupt that is generated each time the converter signals that a sample is ready via the Data Ready line. Figure 4.9 shows the contents of the DSP buffer containing the A/D converter output as viewed within the VisualDSP++ plot window.

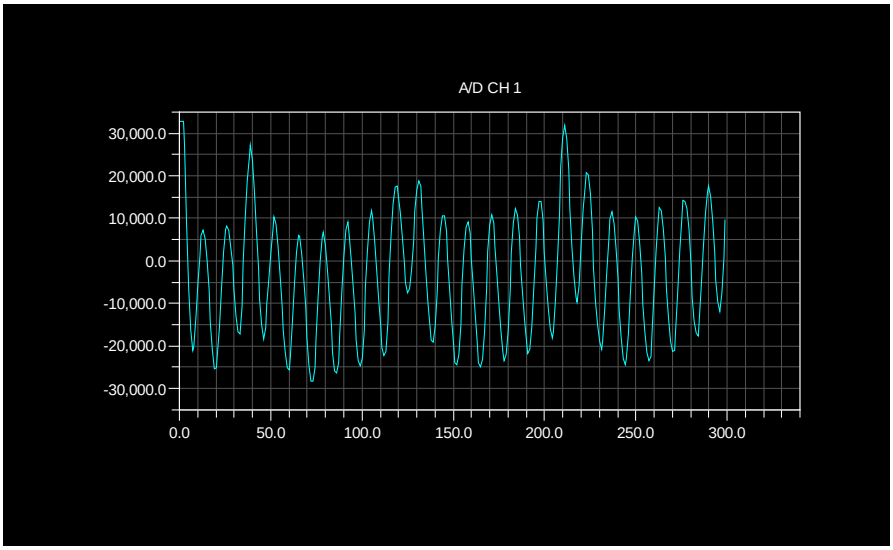

Figure 4.9: VisualDSP++ plot window with A/D converter output as received into the DSP

The 200 Hz acoustic signal can clearly be seen without data drop-outs as well as some remaining 60 Hz interference. The signal level was increased and decreased to demonstrate clipping and to evaluate any DC bias.

4.2 EMBEDDED DSP

The BlackFin 538F DSP demanded a considerable portion of the node checkout. The transceiver connection over SPORT interface, A/D connection over SPI interface, JTAG programming port operation, external voltage regulation, and internal flash memory programming for bootable program storage all required tests. After confirmation that the +/- 5, +3.3, and +1.8 supply voltages were correct, a connection was successfully established over the Analog Devices USB-ICE JTAG programmer. A test program was written to handle DSP configuration and device driver setups and to begin interface testing. API function calls are available to configure the core clock speed, set the core voltage by changing the duty cycle of a PWM output, and to configure the ports. SPORT0 is used to transmit data over the telemetry link, SPORT1 is used to receive

telemetry data, and SPORT2 is used only to source a master clock for the transceiver. SPI0 is used to read data from the delta-sigma A/D converter. An 8 MHz silicon oscillator, MAX735, supplies the core clock signal which is then multiplied inside the DSP to approach the 500MHz maximum operating speed. DSP power consumption is primarily controlled by variation of the core voltage and the clock speed.

$$\text{Power Savings Factor} = \frac{f_{CCLKRED}}{f_{CCLKNOM}} \times \left(\frac{V_{DDINTRED}}{V_{DDINTNOM}}\right)^2 \times \left(\frac{T_{RED}}{T_{NOM}}\right)$$

where the variables in the equation are:

- $f_{CCLKNOM}$ is the nominal core clock frequency
- $f_{CCLKRED}$ is the reduced core clock frequency
- $V_{DDINTNOM}$ is the nominal internal supply voltage
- $V_{DDINTRED}$ is the reduced internal supply voltage
- T_{NOM} is the duration running at $f_{CCLKNOM}$
- T_{RED} is the duration running at $f_{CCLKRED}$

The power savings factor is calculated as:

$$\%\ \text{Power Savings} = (1 - \text{Power Savings Factor}) \times 100\%$$

Figure 4.10: DSP power savings calculation, Analog Devices ADSP-538F data sheet

Figure 4.10 above shows the calculation for power savings attributable to voltage and clock speed. Unfortunately, use of the built in functions for varying the core voltage PWM control signal did not work. No error codes were returned, however the PWM duty cycle did not change as directed. The overall DSP power consumption could likely be lowered after resolution of the control function.

DSP code can be compiled and built as an executable for debugging and general testing. When the code is ready for testing without the JTAG connection it can be built as a loader file, downloaded, and flashed into the DSP internal memory. This functionality was very useful and worked well with the BF538F DSP.

4.3 Power Distribution

Array power was supplied by an Agilent N5749A 100V 7.5A DC power supply. The array supply voltage was set at 72V and was switched down by each node to +/-5 and 3.3 volts by Calex DC-DC converters. The 1.8 volts required by the A/D is supplied by a Linear Technologies LT3009ESC8 linear voltage regulator tapped off of the 5 volt supply. The total node power consumption was measured at approximately ¾ of a watt.

4.4 Timing

Acoustic sample clock timing was generated in the recorder rack by an Agilent 33220A function generator and a MAX3292 RS422 converter IC. Each node in the array is connected to the same clock signal to achieve simultaneous sampling, neglecting propagation delay. The MAX3292 can support over 300 receivers all tied onto the same transmission line without loading due to its high input impedance. A matching MAX3292 is located at each node to convert the differential clock back to single ended. The delta-sigma A/D converter output data rate is 1/512 that of the input clock rate. To achieve 4 kHz of acoustic bandwidth, the data must be sampled at minimum of 8 kHz which would require a source sample clock of 4.096MHz for this converter. The MAX3292 can drive up to 5MHz signals down 300 meter twisted pair wires without suffering too much attenuation. If longer cable lengths were desired, a reconditioning repeater might be required.

4.5 Telemetry

Incorporating the Dallas Semiconductor DS-3150 transceiver into a complete array design required testing a number of the additional components that are part of the telemetry hardware. The acoustic node connectors and signal termination were an initial concern. With high speed signaling, drastic changes in impedance can cause reflected

energy in the transmission line. A series of tests were performed by connecting a wet pluggable Subconn connector in parallel with a properly terminated 75 ohm RG58 coaxial cable. The results from a time domain reflectometer test are shown below in Figure 4.11.

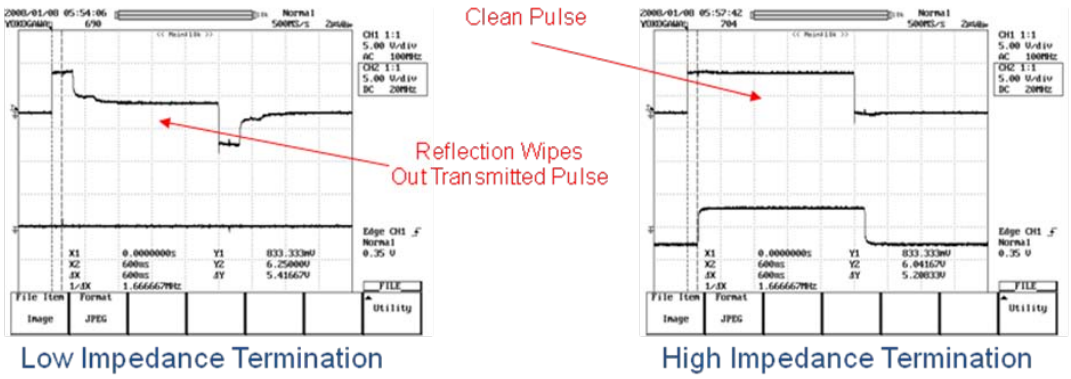

Figure 4.11: Time domain reflectometer tests for parallel node attachment

When the node is attached in parallel through a connector and the overall node input impedance is high, the transmitted pulse travels undisturbed. A low impedance node connection causes considerable reflected energy. A parallel configuration is therefore possible as long as the nodes are connected and high input impedance is maintained. For daisy chained configurations, where the output of any previous node is connected to the input of the next node and so on, it is only necessary to maintain a suitable 75 ohm termination at each node. The recommended transceiver termination maintains this 75 ohm impedance without the need for a high impedance high speed unity gain buffer amplifier that would otherwise be required for the parallel case. The daisy chained configuration also provides signal reconditioning at each node and allows for a solid and stable link between the two transceivers to be maintained. A parallel connected

array requires negotiation of transmit authority by each node over the shared bus. For these reasons, a daisy chained approach was selected for this thesis.

The first step in testing the telemetry was to bench test with manufacturer development kits. Figure 4.12 shows the development kit hardware assembled for the initial telemetry tests, minus the digital oscilloscope used to capture the raw waveforms.

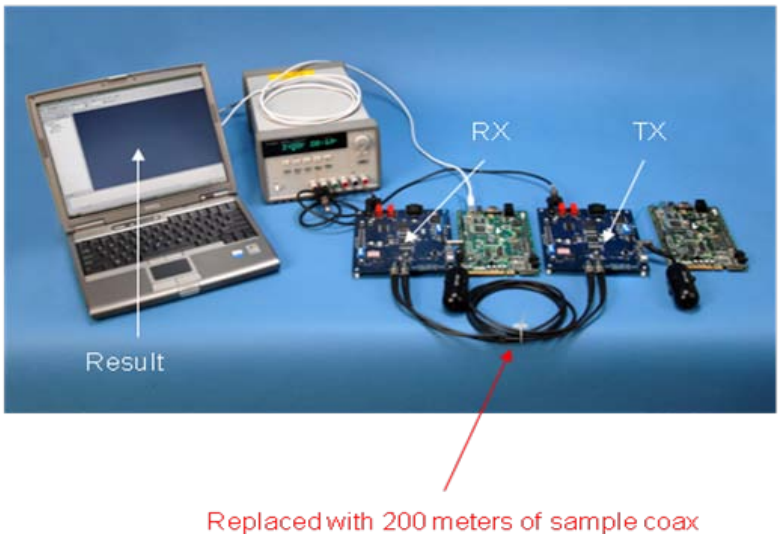

Figure 4.12: DTA telemetry bench test development kit hardware

The BlackFin DSP development kit was connected to the Dallas Semiconductor transceiver development kit using jumper wires to make the SPORT connections. Using VisualDSP++ and the USB JTAG programmer, a sample buffer of data was transferred from one DSP-transceiver pair to another with a sample piece of 75 ohm coax in-between. The known test data was successfully received with 100% data integrity at 31.5MHz. The transceiver master clock is supplied by SPORT 2 for convenience. The clock must be a multiple of the DSP clock and so 31.5MHz was used again for convenience. Figure 4.13 below shows the raw waveforms captured with a Yokogawa 4 channel digital oscilloscope.

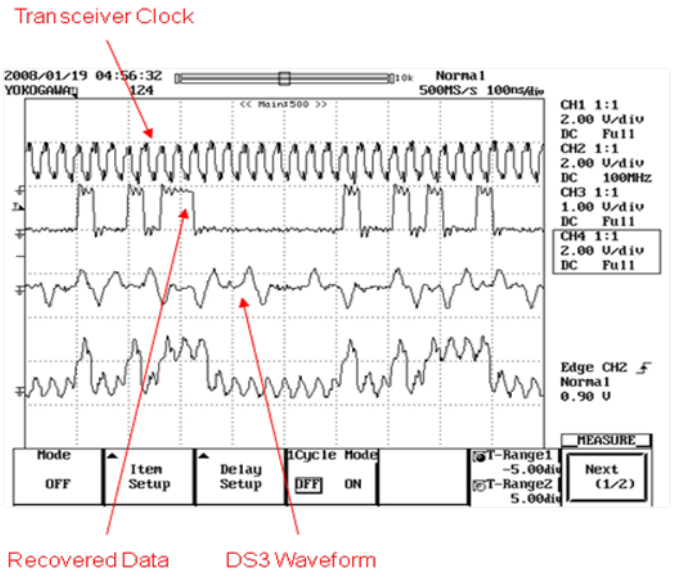

Figure 4.13: DTA telemetry waveforms using development kit hardware

The DSP to transceiver hardware and software interface were validated. After successful tests with simulated processor overhead running in the background, the first prototype was designed and built. As mentioned previously, this version of the prototype was delivered without the DSP installed due to a manufacturing problem. To test the telemetry, the DSP development kit was wired into the prototype. The same series of tests were performed with the new board. Figure 4.14 below shows the transmitted and recovered serial data. At the beginning of each transmitted data packet is a header that is used to identify the beginning of a valid packet. The DSP receive SPORT 1 is configured in a framed slave configuration. A start of frame signal is required to initiate a read sequence. The transceiver does not have an appropriate signal to serve as the frame sync; therefore, the packet header itself was used. A high bit (hex word 0x0001) at the beginning of each packet triggers a frame sync if the transceiver output is wired directly to the frame sync input of SPORT 1. This method proved successful though atypical.

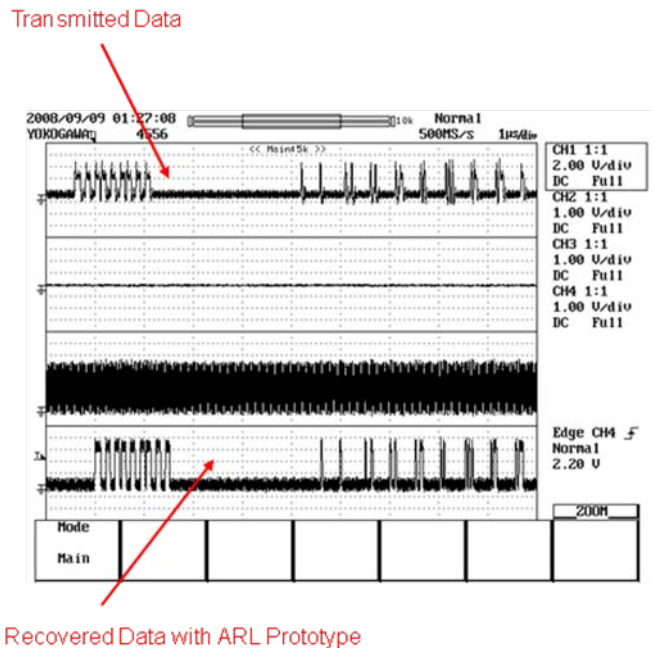

Figure 4.14: DTA telemetry waveforms using prototype version 1 and DSP development kit

The telemetry link can be operated at slower speeds by programming each DSP in the array nodes and in the array interface module (AIM) with the same transceiver master and transmit clock frequencies. Further testing showed that when operated over short lengths of twisted pair wire, the transceivers performed equally as well with 100% data integrity. For arrays with reasonably close element spacing in the tens of meters or less, twisted pair wiring would work well and would be much more attractive than coaxial cable from a cost, size, and weight standpoint.

4.6 Pressure Tolerance Testing

Section 2.10 discusses component selection for pressure tolerant designs. For those components that can be tested or that are not simple ICs, resistors, or ceramic capacitors, they need to be pressure tested individually prior to inclusion in a complete hardware design. This helps prevent poor design decisions early on. A small stainless

steel pressure vessel with an electrical feed-through was available for testing a few of the non-standard components of the prototype. Figure 4.15 shows the pressure vessel setup.

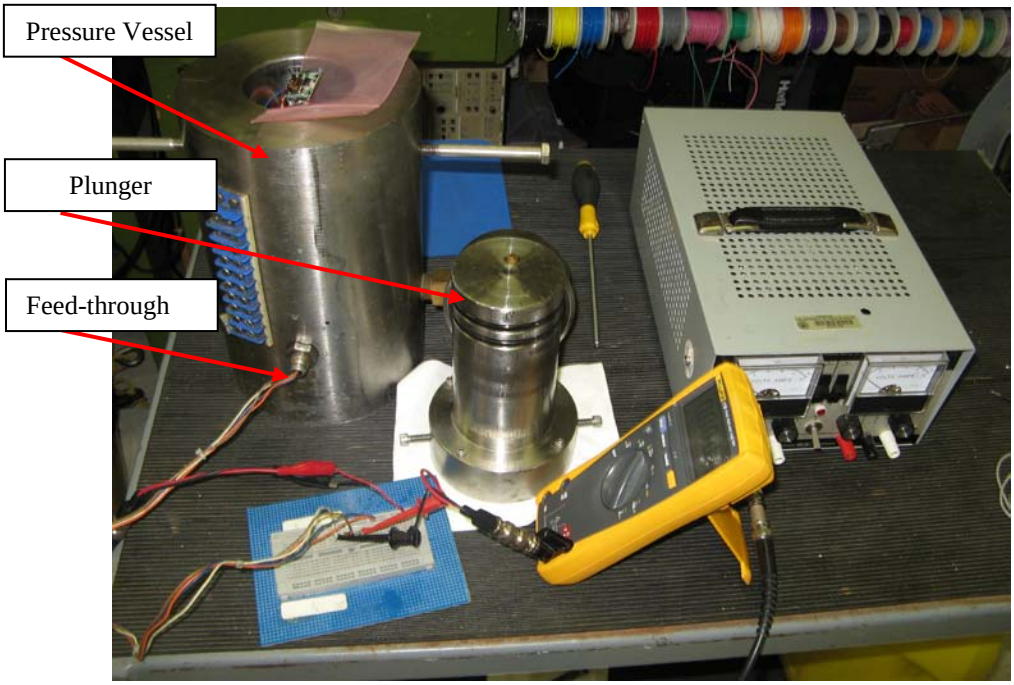

Figure 4.15: DTA prototype component pressure test setup. 68.9 MPa vessel with feed-through.

A large hydraulic press is used to compress the plunger into the pressure vessel. A gauge located in the sidewall provides pressure readings. The feed-through allowed the Calex power supplies to be tested under power and with a load connected. Castor oil was used inside the vessel since it is a good dielectric. The power supplies were first encapsulated in a low viscosity Stycast brand epoxy with a relatively high thermal conductivity. Both the +3.3V and +5V supplies passed a 68.9 MPa pressure test.

Figure 4.16: Upper: Calex DC-DC supply wired into the pressure vessel. Lower: Hydraulic Press.

Figure 4.16 above shows the Calex supply wired into the pressure vessel as well as the hydraulic press setup used to add the pressure. The telemetry transceiver transformers needed to be tested as well. Figure 4.17 shows a cross-section of the transformer after being sawed in two and the transformer wired into the pressure vessel for testing. The absence of air voids from the cut-away was a positive indicator that the transformer should be pressure tolerant and it did operate correctly all the way up to 68.9 MPa.

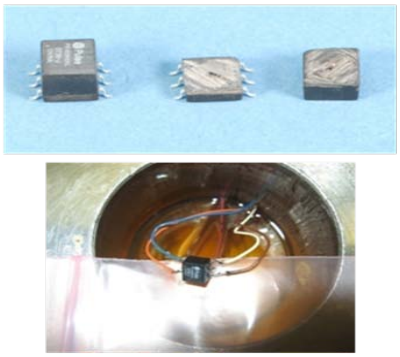

Figure 4.17: Upper: Transformer cross-section. Lower: Transformer wired into pressure vessel.

The effect of pressure on the coaxial cable impedance was also of interest, especially for consideration of arrays in excess of 300 or 400 meters. Compression of the coaxial cable dielectric will cause a corresponding change in the characteristic impedance, which can be defined according to the following relations

$$Z_0 = \sqrt{\frac{L}{C}} \tag{4-1}$$

$$C = \frac{7.38 * \varepsilon}{\log\left(\frac{D}{d}\right)} \tag{4-2}$$

$$L = 0.140 * \log\left(\frac{D}{d}\right) \tag{4-3}$$

Z_0 is the characteristic impedance, C = capacitance per foot, L = inductance per foot, D = dielectric outer diameter, d = dielectric inner diameter, and ε is the dielectric constant. Figure 4.18 below shows a diagram of a typical coaxial cable.

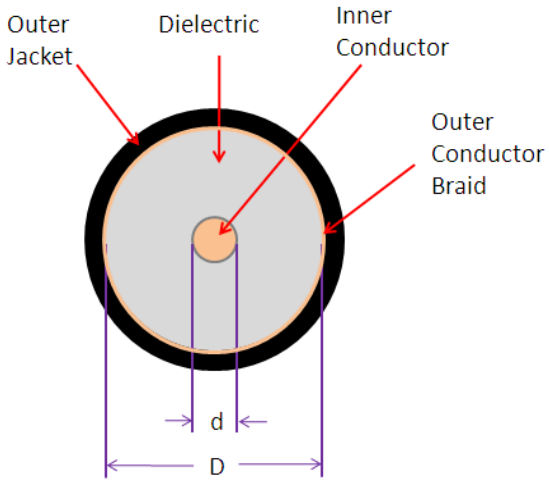

Figure 4.18: Coaxial Cable Diagram

As the cable compresses, the thickness of the dielectric will decrease due to changes in the outer diameter *D*. This should cause the inductance to decrease and the capacitance to increase, resulting in a slight decrease in characteristic impedance due to the geometry change. Compression of the dielectric could cause a change in the dielectric constant as well. In the absence of a vector impedance analyzer, a propagation speed measurement approach was taken in order to evaluate these parameters while under pressure. A 28.8 meter, 94.48 feet, section of 75 ohm RG-59 coaxial cable from Falmat Cable was passed into a large 20.6 MPa rated pressure vessel at ARLUT via two custom penetrators with hard-rubber cores as shown below in Figure 4.19.

- Measured the effect of pressure on coaxial cable impedance
- Falmat Cable - 75 Ohm RG-59
- Medium Density Polyethylene dielectric
- Dielectric constant of 2.2
- Pressurized to 3,000 psi
- Velocity factor changed yielding a new dielectric constant of 2.4, consistent with high density polyethylene.
- Measured compression yielded a new impedance of 68 ohms.
- Transceiver test with 50 ohm coax showed equivalent performance.
- Vendors can provide PTFE dielectrics to minimize compression.
- Cortland Cable claims 3 ohm variation at 10,000 psi with PTFE.

Figure 4.19: Coaxial cable pressure test setup in ARLUT's 20.6 MPa vessel

The RG-59 cable dielectric material was made of medium density polyethylene with a published relative dielectric constant of 2.2. An AIM brand antenna tester was connected to one end while one of three different impedance terminations was connected to the

opposite end. A test frequency of 50MHz was selected and a pressure profile from 0 to 20.6 MPa was run. The AIM tester provides a measurement of the transmission line length based on an assumed propagation velocity. A propagation velocity of 0.66 times the speed of light was used throughout the testing. At ambient pressure, the tester accurately measured the cable at 94.5 feet. At 20.6 MPa, the tester measured the cable at 95.3 feet. The velocity factor is likely changing due to the compression, which introduces error given that the tester is still using a 0.66 factor. Using the following relation where c is 3e10 m/s, Δt is the round trip travel time, and L is the cable length,

Error! Bookmark not defined. $$0.66c\Delta t = 2L \tag{4-4}$$

the elapsed round trip travel time can be estimated based on the measured length. At 0 MPa the travel time was 2.9102e-7 seconds and at 20.6 MPa the travel time was 2.9348e-7 seconds. The actual propagation velocity at 20.6 MPa can now be estimated using equation 4-5.

$$v_p = \frac{2L}{\Delta t} \tag{4-5}$$

The propagation velocity at 20.6 MPa should actually have been 1.962e8 m/s which yields a velocity factor of 0.654 instead of 0.66. The propagation velocity is useful in determining the change in dielectric material properties through the following equation where β is the propagation constant, μ is the magnetic permeability, ε is the dielectric constant, and $\frac{\chi_{mn}'}{a}$ represents the propagation mode.

$$\beta = \sqrt{\omega^2 \mu\varepsilon - \left(\frac{\chi_{mn}'}{a}\right)^2} = \frac{\omega}{v_p} \tag{4-6}$$

At 0 MPa, we know the propagation velocity and the frequency of the test signal (50MHz). It is then easy to solve for β, which is 1.5866. Using equation 4-6, $\frac{\chi'_{mn}}{a}$ can be solved for and is found to be 0.101439. Using the same relations, β at 20.6 MPa must be 1.6007. Assuming that $\frac{\chi'_{mn}}{a}$ is constant, ε at 20.6 MPa can be solved for and is found to be 2.1465e-11. Since $\varepsilon = \varepsilon_0\varepsilon_R$ where ε_0 is the free space dielectric constant, the relative dielectric constant is now 2.42. Interestingly, the new compressed dielectric constant is very close to the published values for high density polyethylene. After removal of the coaxial cable from the pressure vessel, the polyethylene dielectric maintained its compressed thickness. The change in thickness could then be measured and the new characteristic impedance could be calculated when combined with the new dielectric constant. From equations 4-1, 4-2, and 4-3, the impedance was estimated to have changed from 75 ohms to 68.5 ohms at 20.6 MPa. In order to extrapolate these values to 68.9 MPa, a few assumptions were made. Table 4-1 contains the estimated change in impedance, Z2, as a function of dielectric compression percentage.

Diel. Comp.	D2	d2	C2(pF)	L2(uH)	Z2(ohms)	ΔZ - Ohms	ΔZ-%
0.01	0.1940	0.03	22.96	0.11	68.50	3.45	4.80
0.02	0.1921	0.03	23.09	0.11	68.10	3.84	5.34
0.03	0.1901	0.03	23.23	0.11	67.71	4.24	5.89
0.04	0.1882	0.03	23.36	0.11	67.31	4.64	6.45
0.05	0.1862	0.03	23.51	0.11	66.90	5.05	7.01
0.06	0.1842	0.03	23.65	0.10	66.49	5.46	7.58
0.07	0.1823	0.03	23.80	0.10	66.08	5.87	8.16
0.08	0.1803	0.03	23.95	0.10	65.66	6.29	8.74
0.09	0.1784	0.03	24.11	0.10	65.24	6.71	9.33
0.10	0.1764	0.03	24.26	0.10	64.81	7.14	9.92

Table 4-1: Coaxial Cable Impedance Change with Depth due to Pressurization

It is reasonable to assume that the dielectric will likely not follow a linear compression curve. As the dielectric becomes denser, it will likely see less compression per increase in pressure. Table 4-1 indicates the change in impedance for a given range of dielectric compression from 1% at 20.6 MPa to 10% at an unknown pressure. If 20.6 MPa only imparts 1% compression, it is reasonable to assume that 68.9 MPa would fall under the 10% range. It is also worth noting that the calculated impedance using the equations presented in this section for the cable at 0 Pa came to 72 ohms. Therefore, the impedance changes represented in Table 4-1are relative to the calculated 72 ohm value.

Pressure test results for the coaxial cable showed that the impedance would change as a function of depth by as much as 10 ohms. The 75 ohm RG-59 was replaced by a 50 ohm piece of RG-58 and the telemetry was re-tested. For a 100 meter section, the performance was equally good with both cable types. While there may be some degradation in signal quality over even longer cable lengths, for most practical applications, even a drastic 25 ohm variation did not cause any real problems for the transceivers. Oceanographic cable manufacturers offer cables with a polytetrafluoroethylene (PTFE) dielectric to minimize compression and claim as little as 3 ohms of impedance change at 68.9 MPa to further minimize the concern.

CHAPTER 5 CONCLUSIONS AND DISCUSSIONS

Pressure tolerant acoustic receiving line arrays with digital telemetry can be designed and built to suite a broad range of applications. This allows for smaller form factor arrays with larger element counts compared with analog array designs. In order to understand the impact that each component has on the overall design, this thesis investigated the complete development process.

The objective of designing a pressure tolerant digital telemetry hydrophone array was met based on a number of factors. A per element power consumption of ¾ watts was achieved. Digital telemetry over long distance coaxial or twisted pair copper was demonstrated using COTS transceivers. The hydrophone element, digitizing A/D, and telemetry electronics were pressure tested successfully to 20.6 MPa encapsulated in urethane using a precise pre-treatment process to eliminate air gaps. The delta-sigma A/D converter is capable of at least 10 kHz sample rates for clean 4 kHz of acoustic bandwidth. The hydrophone amplifier was designed with a gain of 72 dB in order to achieve a useful receive range of 45 to 135 dB re 1µPa for deep ocean applications. Unfortunately, the amplifiers self noise was too high resulting in a noise floor of approximately 55 dB at 100 Hz, which is well above SS0 ambient noise levels. Furthermore, when operating at such high gain levels, the AD627 instrumentation amplifier used only has a flat response out to 1 kHz. The two stage amplifier design incorporated a single ended section which made the design susceptible to 60 Hz noise. This was overcome using a faraday cage for laboratory testing. Given the nature of the required testing for this thesis, these limitations did not pose a problem and alternative designs were recommended. The telemetry objective of accommodating 300 nodes, each operating at 8 kHz (16 bit) data rates was almost realizable using two data buses. This

splits the required 40Mbs bandwidth into two separate buses operating at 31.5 MHz, which is necessary to allow for data packet and link overhead. In a daisy chained configuration, each node's transceiver performs a hardware loopback and re-transmits the previous node's data on down the array with very little delay. The measured delay of 0.3 microseconds at each node results in a total delay of 0.22 milliseconds for a node at the beginning of the array to transmit its data all the way through. If each node is allowed the same amount of time to send its packet, then 300 nodes will require 66.6 milliseconds to offload their data packets. This only allows for a sample rate at each node of 3575 Hz and requires each node to buffer 250 samples per packet. Splitting the array into two data buses will double the bandwidth and allow for just over 7 kHz sample rate. This does not meet the original design goal of accommodating 300 modes on one telemetry bus at 8 kHz sample rate, but does come close with two buses which is desirable for redundancy anyway.

While a two channel prototype hydrophone array was built to allow for telemetry testing, only a single channel was encapsulated in urethane and underwent in water acoustic testing due to time and budget constraints. For each hydrophone node, an amplifier was designed to map the hydrophone output into the input range of a 16 bit delta-sigma A/D converter. Data samples were buffered by a BlackFin 538F DSP and then transmitted via digital telemetry over coaxial cable inside a prototype array cable. The acoustic node was supplied with 72 volts DC from a rack-mounted data acquisition system along with a differential sample clock that is intended to drive all array elements simultaneously. Each node switches the primary voltage down locally to the required +/5V and +3.3V so that current draw by the array is minimized reducing resistive losses. The array interface consisted of a matching telemetry transceiver and DSP combination

interfaced to a National Instruments PXI form factor CPU and high speed digital I/O board. Data was offloaded from the array over a parallel I/O connection.

Telemetry testing was successful over coaxial cable 100 meters in length and is designed to operate over 385 meter long sections without requiring any reconditioning. The transceivers were also found to tolerate cables with impedances below 75 ohms. Successful telemetry tests were performed with 50 ohm coaxial cable as well as 10 meter sections of twisted pair wiring providing multiple options for arrays with short element spacing.

A daisy chain configuration was recommended to simplify telemetry transceiver operation and control. Each element receives then re-transmits to its neighbor and so on. The transceivers have built in "loop-back" capability that allows for extremely low latency between reception and re-transmission of received signals without the need for local processor involvement. The local processor sniffs incoming data and decides if a response is warranted.

Test software was written for both the National Instruments data recorder running LabVIEW and the acoustic element DSPs using Analog Devices VisualDSP++ IDE. A basic command and response packet set were defined to accomplish the prototype testing. The data recorder, array interface module (AIM), sample clock generator, array power supply, array cable, and prototype DTA node were all configured for continuous recording. A series of bench tests were performed to evaluate the performance of the telemetry system.

Prior to construction of the prototype node, an acoustic model was constructed using the selected HTI-94-SSW hydrophone, an instrumentation amplifier, and the desired PCB form factor. Free-Field Voltage Receive Sensitivity Response data as well as horizontal and vertical plane directivity patterns were measured to confirm an

omnidirectional response and flat sensitivity from 10Hz to 1kHz. Upon completion of the prototype node, a final receive sensitivity response was measured in ARLUT's large FIR test tank. The data was collected through the telemetry system and was generated using a NUWC J-9 source and reference hydrophone. A fully differential amplifier design was recommended to minimize 60 Hz electronic noise interference which required the use of a Faraday cage for most lab testing.

Pressure tolerant component selection was addressed and individual components of the DTA nodes were tested to 68.9 MPa. An analysis of the change in impedance for coaxial cable due to high pressure exposure was presented along with laboratory test data. A discussion on printed circuit board preparation was given for eliminating air pockets in standard board designs that will cause failures at depth if simply encapsulated in urethane without pre-treatment. The final prototype element was pressure tested successfully to 20.6 MPa. A 68.9 MPa pressure test was pending facility availability at the time this thesis was written.

APPENDIX A DIGITAL TELEMETRY ARRAY NODE SCHEMATICS

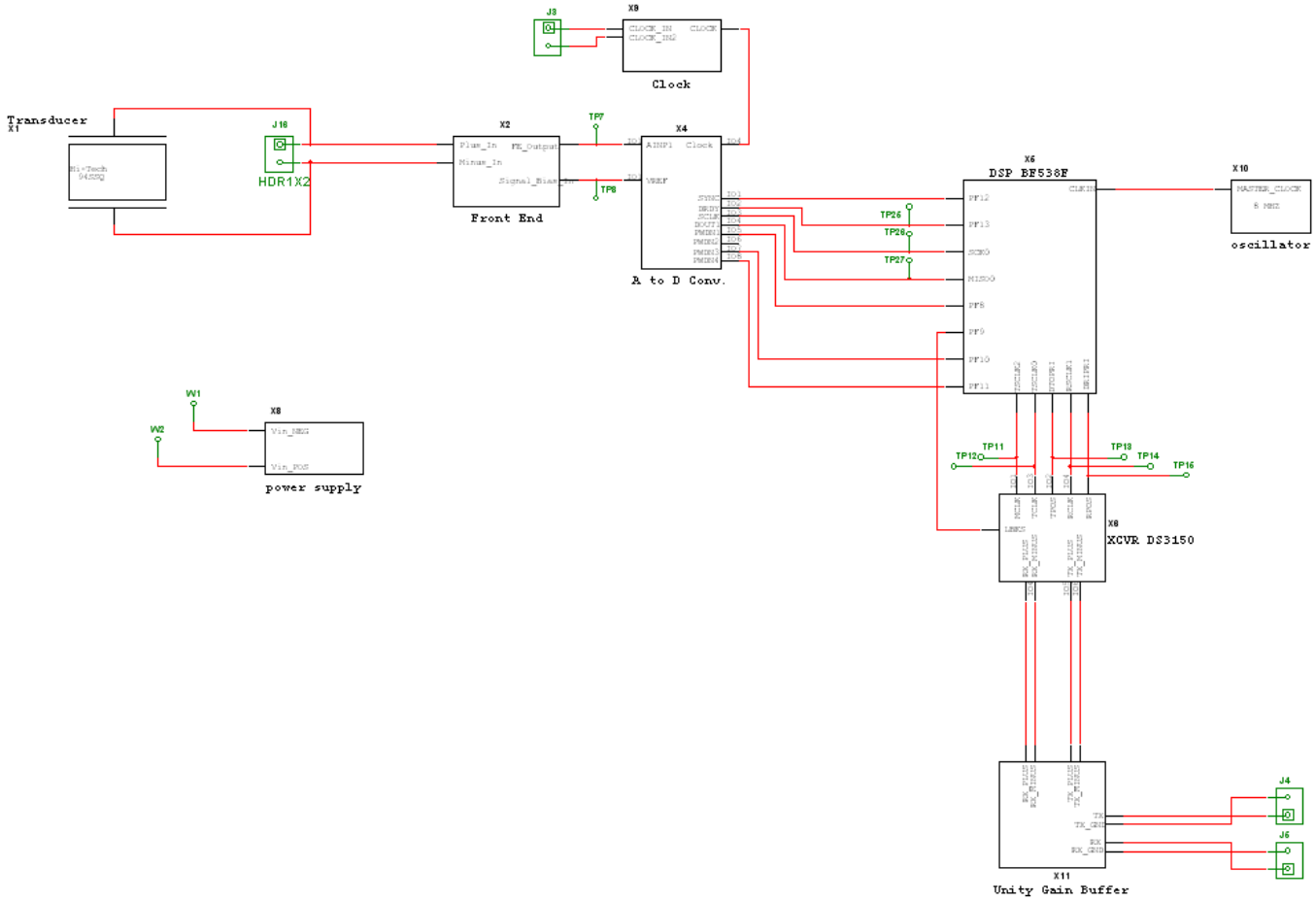

Figure A.1: DTA Node Schematic

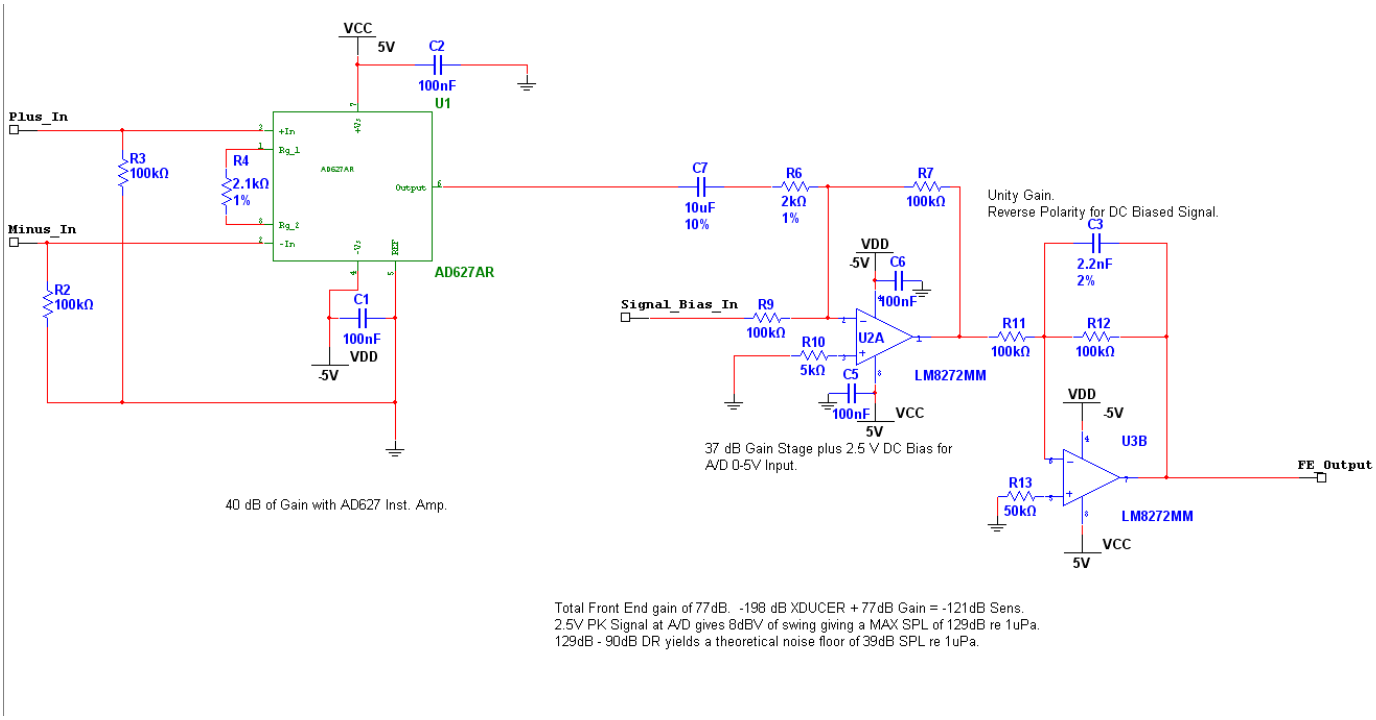

Figure A.2: DTA Node Front End Amplifier Schematic

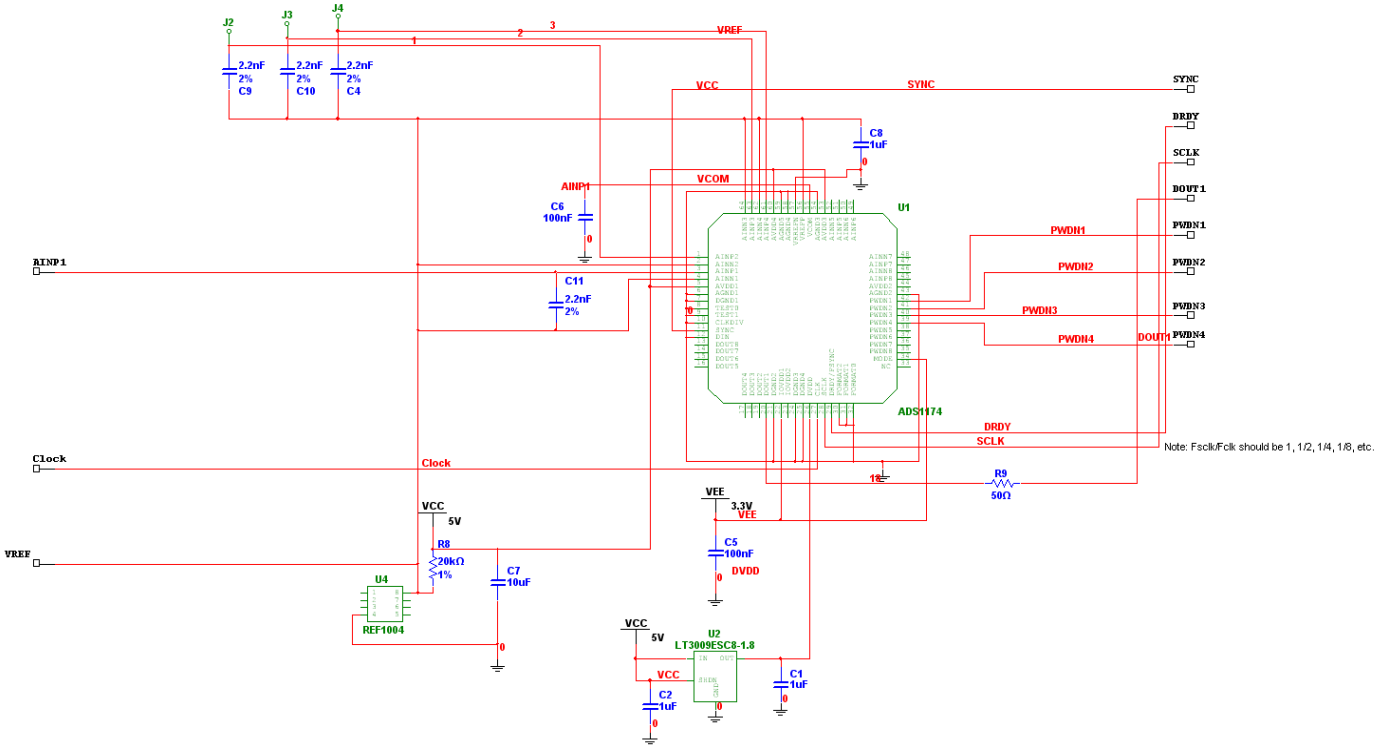

Figure A.3: DTA Node A/D Schematic

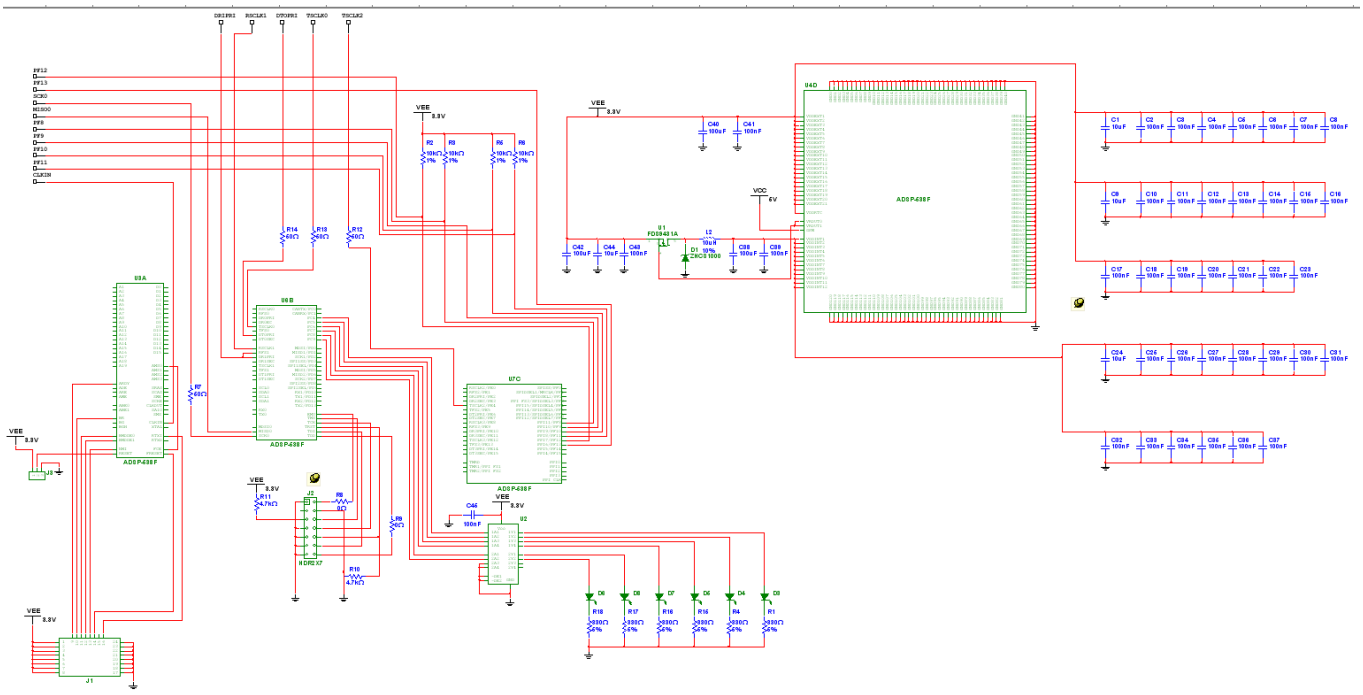

Figure A.4: DTA Node DSP Schematic

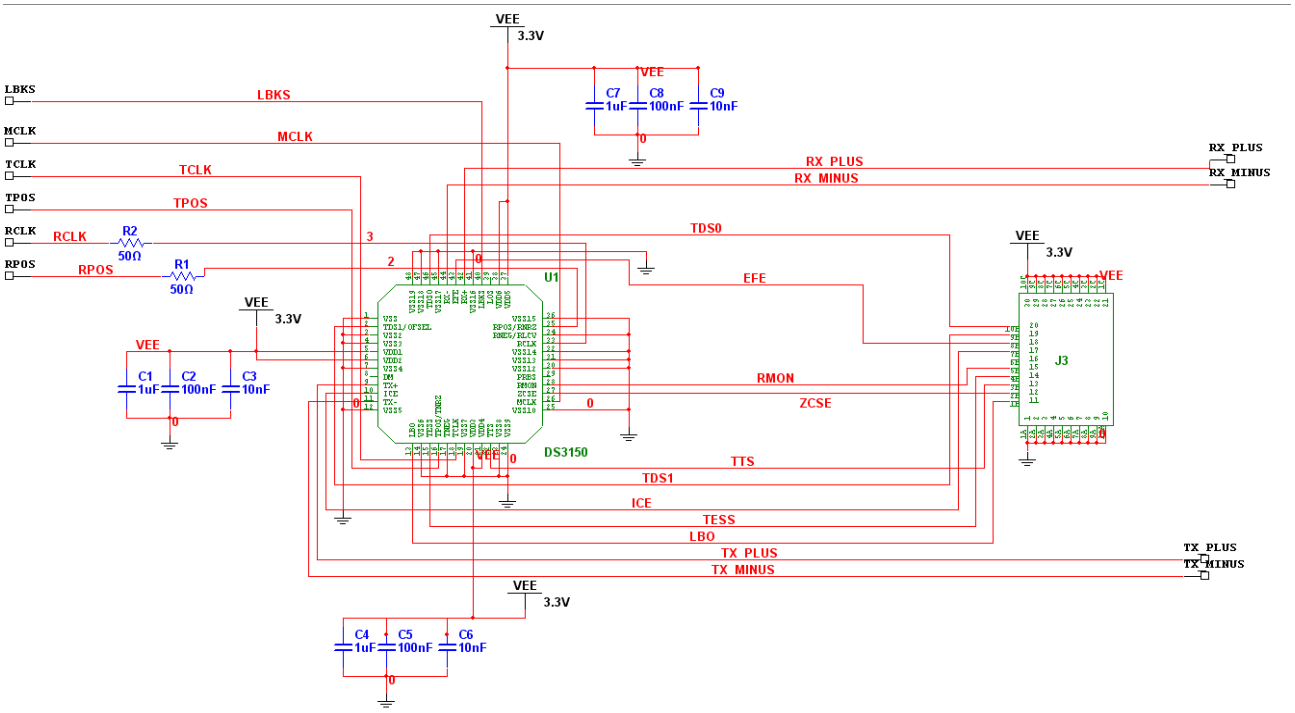

Figure A.5: DTA Node XCVR Schematic

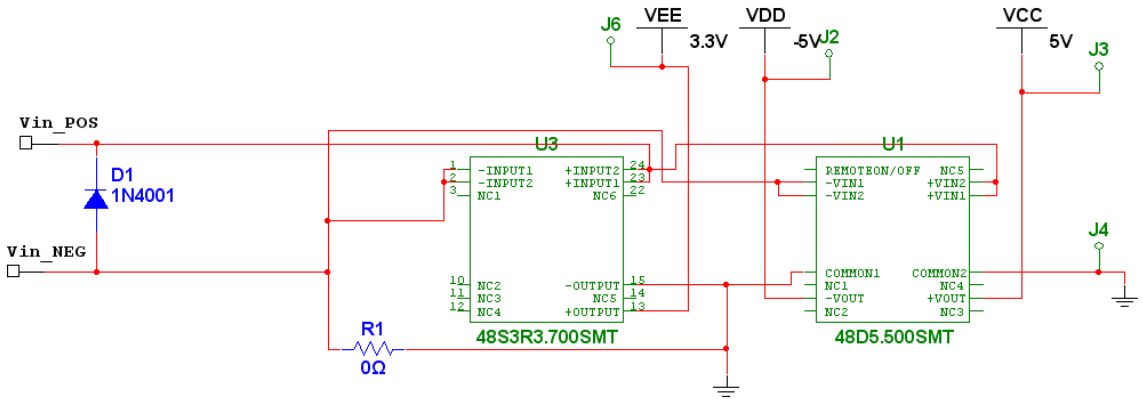

Figure A.6: DTA Node Power Supply Schematic

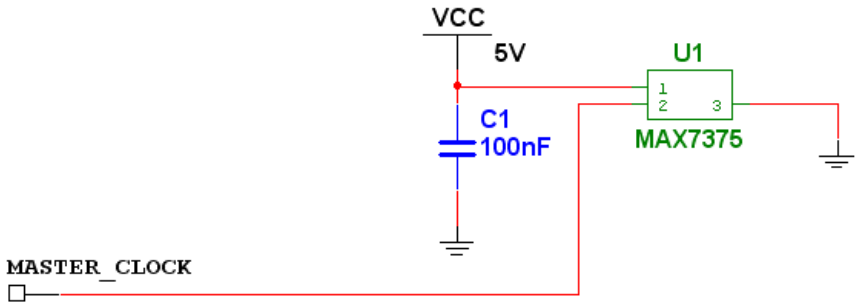

Figure A.7: DTA Node Silicon Oscillator Schematic

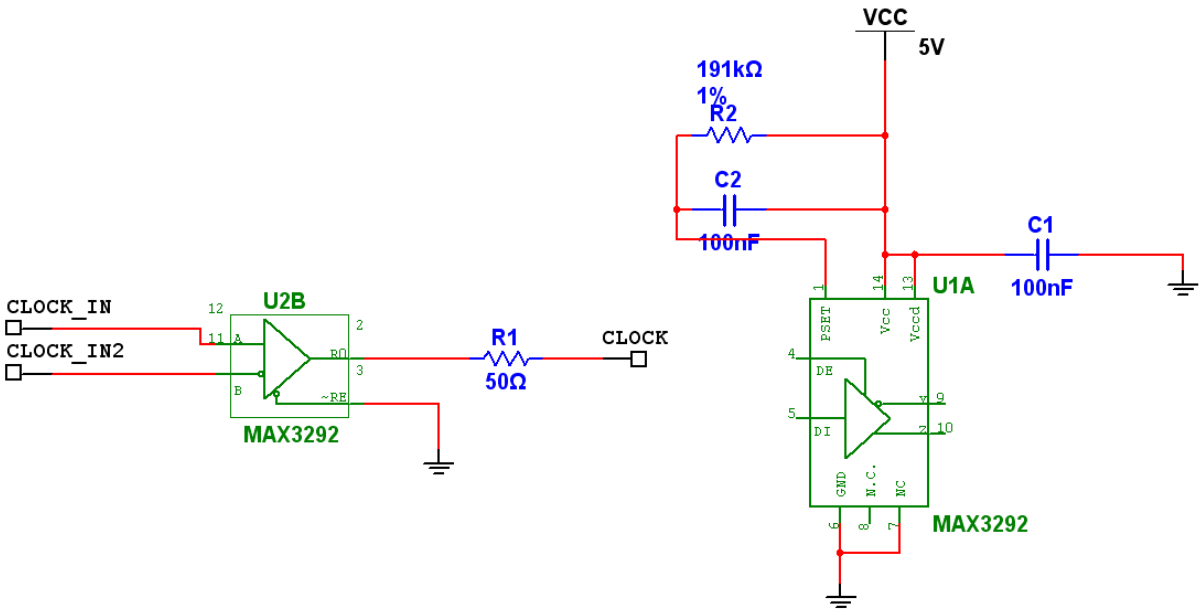

Figure A.8: DTA Node Sample Clock Recovery Schematic

APPENDIX B ARRAY INTERFACE MODULE CONNECTION DIAGRAM

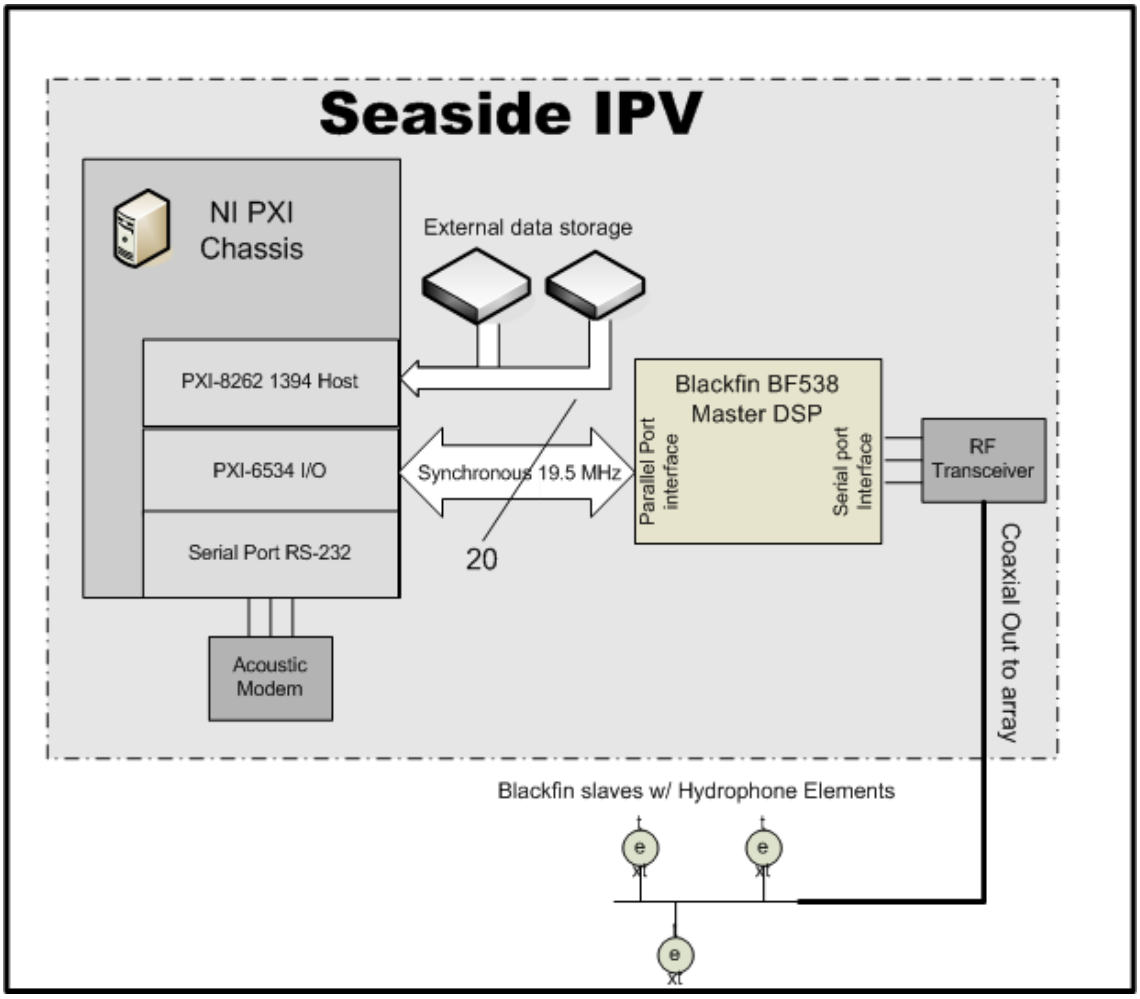

Figure B.1: Overall System Interconnect Diagram

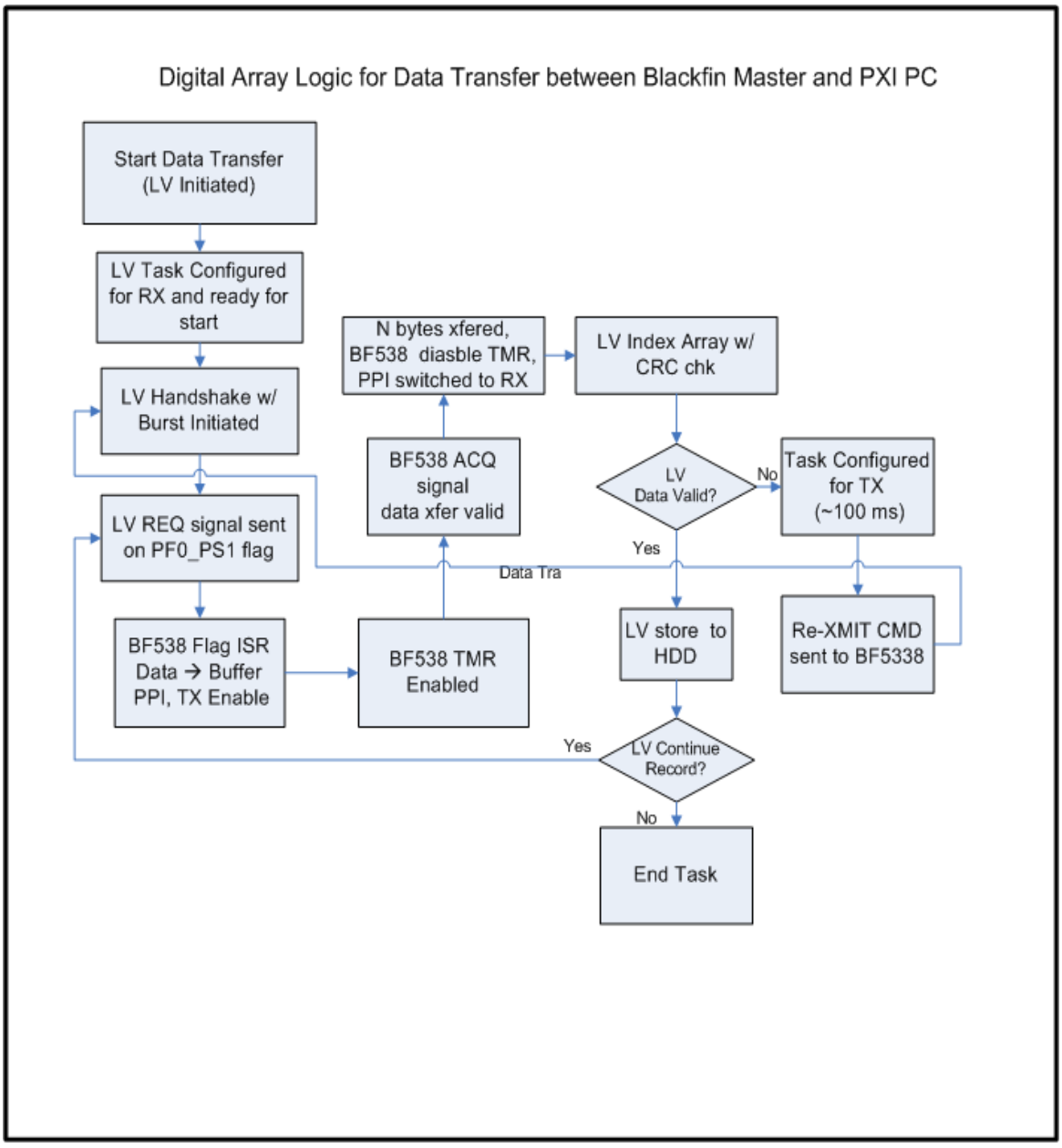

Figure B.2: Logic Diagram for Data Transfer Between AIM and PXI Recorder

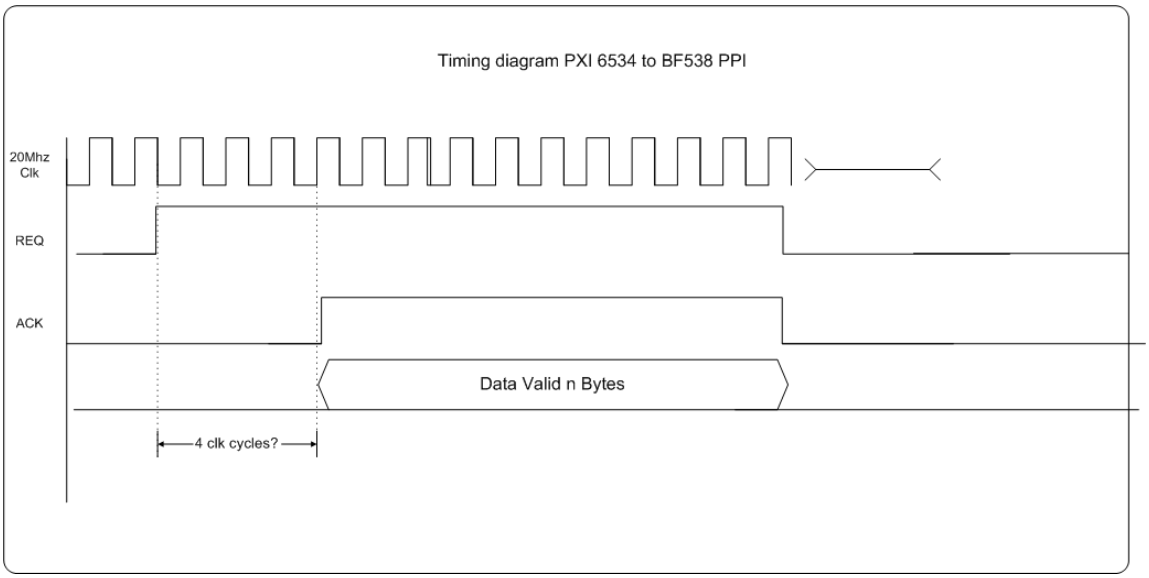

Figure B.3: PXI Recorder to AIM PPI Interface Timing Diagram

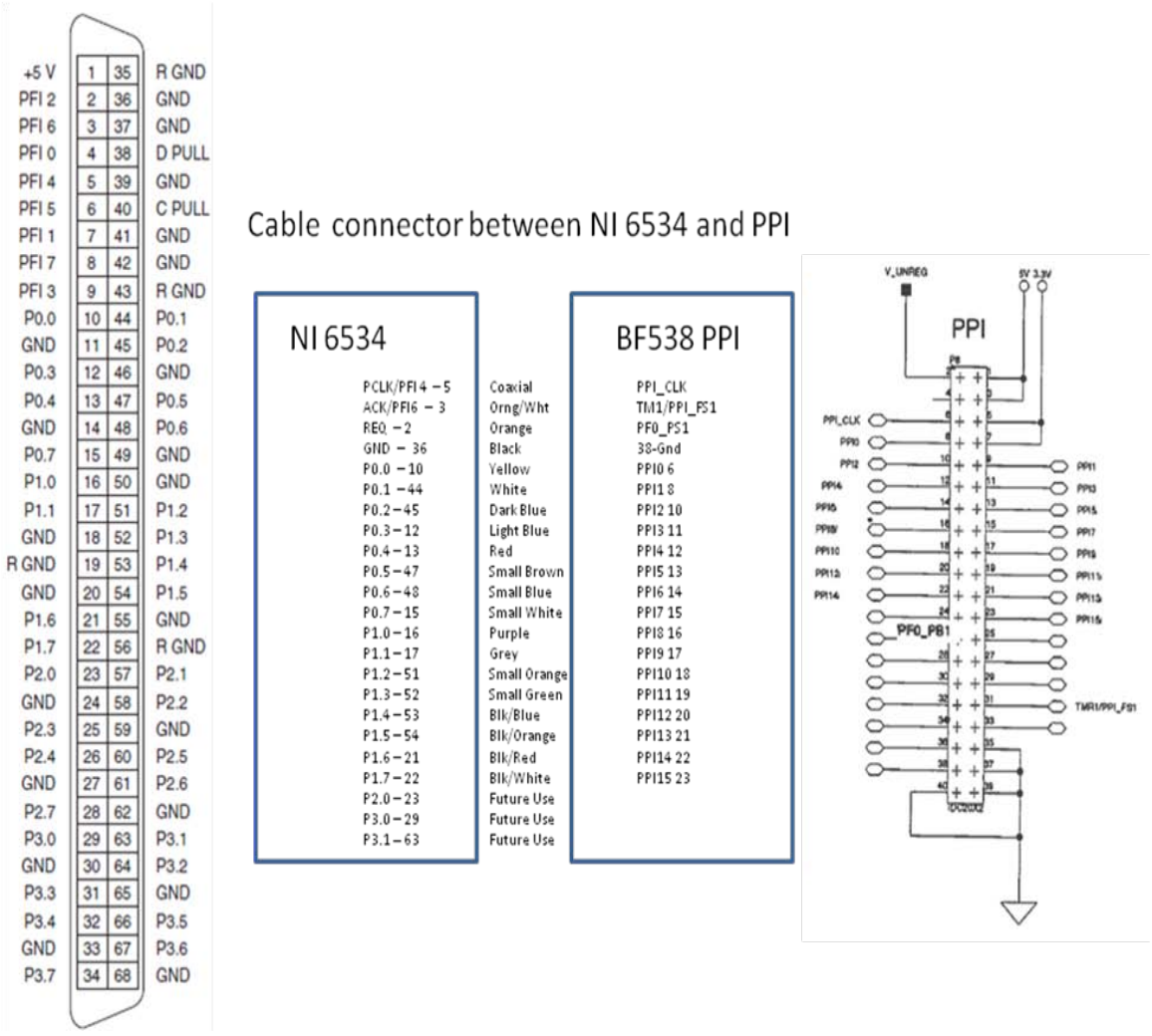

Figure B.4: PXI Recorder to AIM PPI Connection Diagram

APPENDIX C ARRAY TOPOLOGY & TELEMETRY TIMING DIAGRAMS

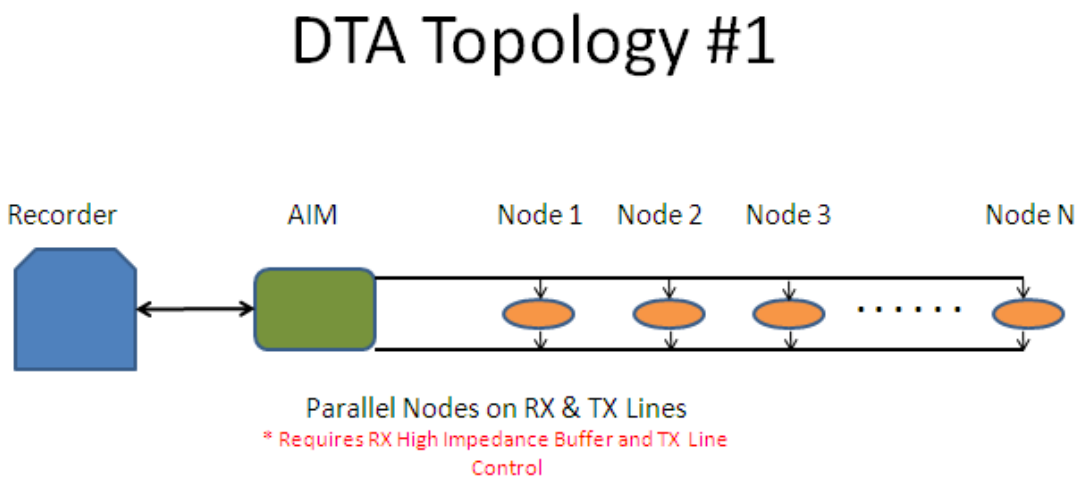

Figure C.1: Parallel connected array topology

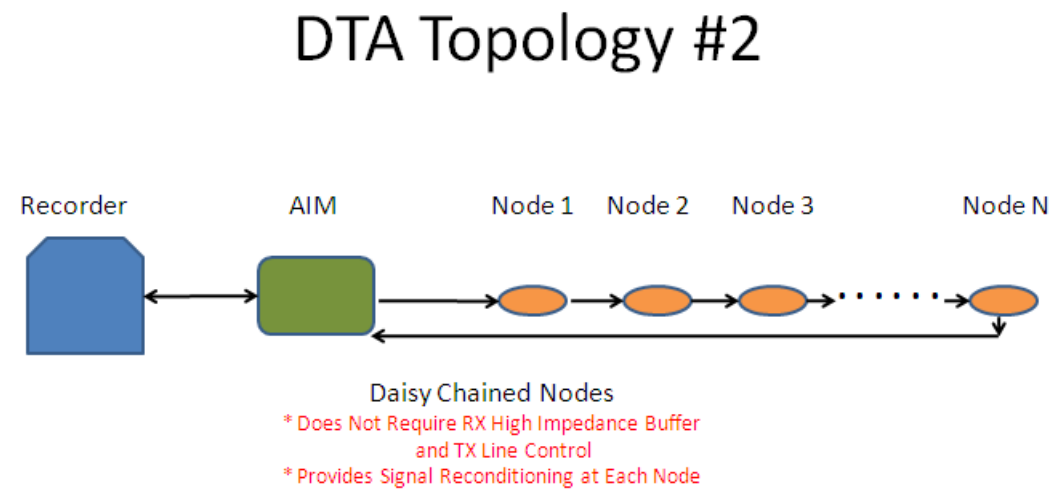

Figure C.2: Daisy chained array topology

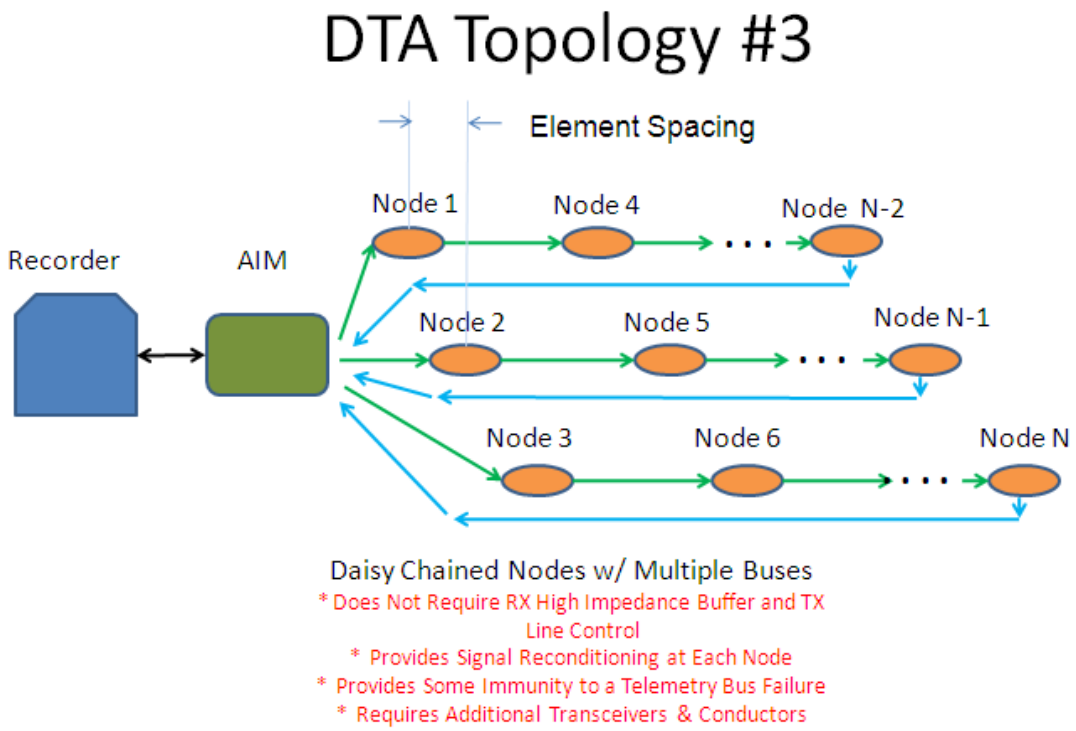

Figure C.3: Daisy chained topology with multiple telemetry buses for fault tolerance

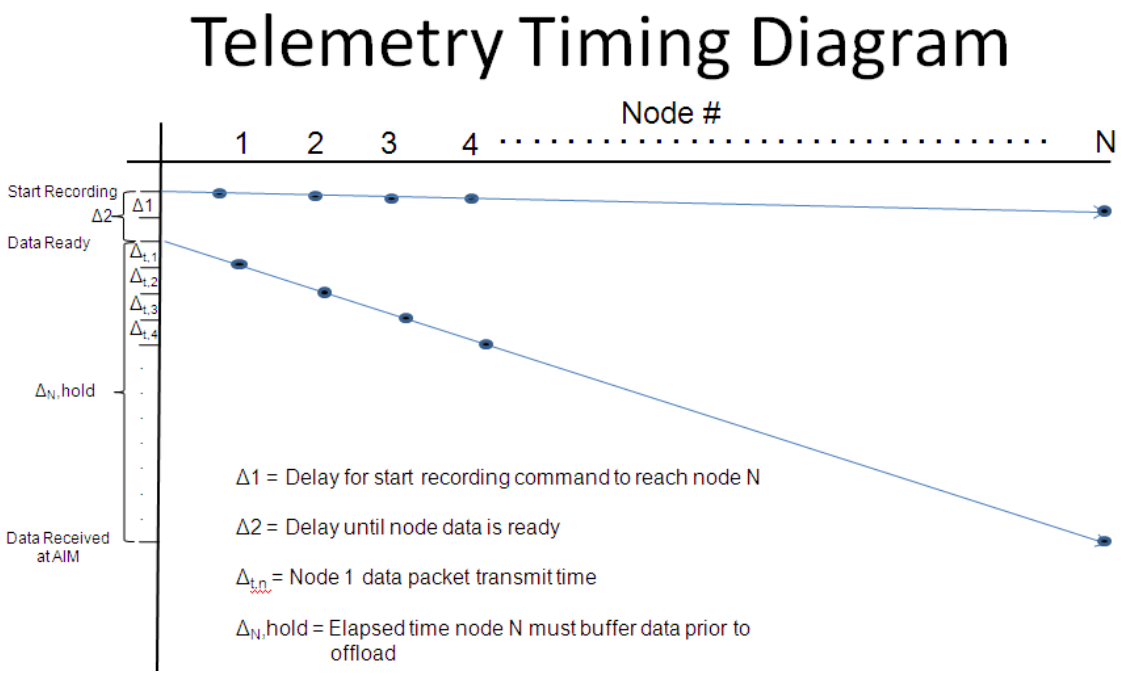

Figure C.4: DTA telemetry timing diagram

List of Symbols

$1\mu Pa$: Standard reference pressure used in underwater acoustics, [10^{-6} Pa]

SPL: Sound pressure level of an acoustic signal, [dB re 1 µPa @ 1m]

G_o: Transducer shunt conductance (1/ohms)

R_h: Resistive component of the transducer equivalent series electrical impedance (ohms)

C_o: Transducer shunt capacitance (Farads)

C_f: Transducer free capacitance (Farads)

C^E: Transducer mechanical compliance

k: Boltzmann's constant (1.381 x 10^{-23} Joule/Kelvin)

T: Absolute temperature (Kelvin)

Δf: Frequency bandwidth (Hz)

$\tan\delta$: Loss tangent

ω: Angular frequency for sinusoidal signals, defined as $2\pi f$ (radians)

$\left\langle p_n^2 \right\rangle$: Mean squared noise pressure (dB re 1µPa)

PCB: Printed Circuit Board

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Vita

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